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CRYSTAL-CONTROLLED PROJECTILE TELEMETRY TRANSMITTER.(U)
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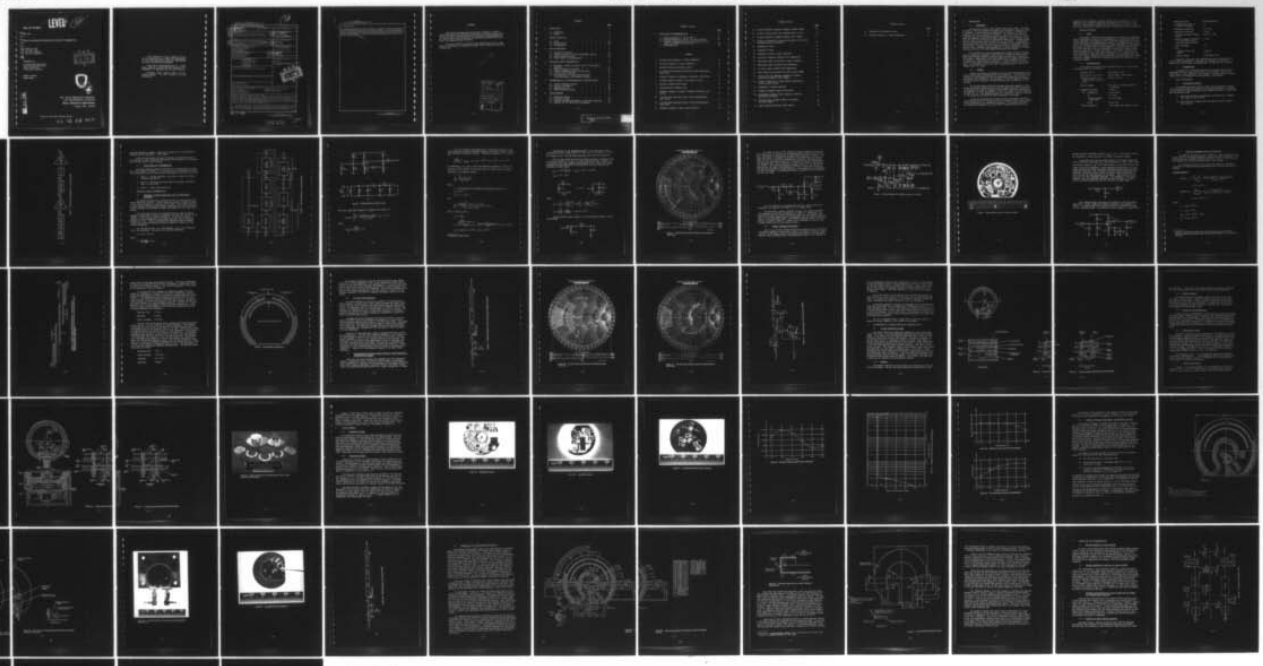

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CRYSTAL-CONTROLLED PROJECTILE TELEMETRY TRANSMITTER

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20. ABSTRACT (*Continue on reverse side if necessary and identify by block number*)

This final report describes the task of redesigning a crystal-controlled projectile telemetering transmitter operating at L-band frequencies. The purpose of the transmitter is for deployment in artillery projectiles to telemeter various performance attributes. Prior efforts on this task included (1) a basic circuit design development by Harry Diamond Laboratories to demonstrate electrical circuit feasibility, excluding packaging ruggedization considerations, and (2) a production engineering program by Motorola's Government Electronics Division.

The approach taken in this effort was based upon the previous work and development of solutions to the complex problems encountered before. These included the combined performance of the oscillator stability, frequency multiplication, microwave stripline filtering, and rf power amplification in a small volume. In addition, the design was to be inexpensive and easily reproducible.

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20. ABSTRACT (Cont'd)

A design was developed that proved to be adequate in satisfying the stability requirements and surviving the high acceleration forces of the artillery environment. The electrical performance problem of the microwave stripline filter was not completely solved, and the proximity effects and resonant cavity responses at the transmitter frequency were determined to be the technical limitations to this design approach. Alternate design approaches have been proposed for solving this serious producibility problem.

FOREWORD

This report describes the effort made to develop a crystal-controlled projectile telemetering transmitter based on previous work done at the Harry Diamond Laboratories (discussed in HDL TR-1564) and on previous work done at Motorola (as discussed in the Motorola Final Report on contract DAAG39-72-C-0074).

The work covered in this report was sponsored by the U.S. Army Materiel Development and Readiness Command, Harry Diamond Laboratories, Adelphi, Md.

CONTENTS

CONTENTS (Cont'd)

FIGURES

FIGURES (Cont'd)

FIGURES (Cont'd)

1. INTRODUCTION

1.1 Background

The technical sponsor, Harry Diamond Laboratories (HDL), initiated an effort at The Johns Hopkins University Applied Physics Laboratory (APL) to redesign a crystal-controlled transmitter to achieve a reproducible design for use in an artillery environment. The transmitter, which was to operate at L-band frequencies, was to be deployed in artillery projectiles to telemeter various performance parameters. HDL previously developed the basic circuit design to demonstrate feasibility. Package ruggedization considerations were excluded from the HDL effort. A production engineering effort was then conducted by the Motorola Government Electronics Division. The goals were not reached because of instability of the initial turn-on frequency with temperature, a limited modulation frequency spectrum, and lack of a cost-effective manufacturing process.

The conversion of previous designs into L-band stripline circuitry and the appropriate redesign of some circuits to minimize tuning adjustments and component selection tailoring were initially set as goals for the program. Additionally, the basic elements of the design were defined to include an overtone crystal oscillator, a power amplifier, a step-recovery diode (SRD) frequency multiplier, a filter, and an output amplifier. The transmitter was to fit into a cylindrical space 1 1/2 in. in diameter and 1 in. long.

1.2 Summary

Efforts to achieve a transmitter with the desired performance within the initial space limitations were not successful. The electrical performance of the stripline filter was compromised within the confines of the housing wall dimensions. The proximity of the SRD times-10 frequency multiplier to the filter on the same substrate also contributed to this problem.

The initial design included a marginal mechanical support for the ceramic substrates that did not survive the high-acceleration environment. An evaluation of possible changes in size revealed that the limitation on the diameter could not be violated but the 1 in. length could be increased by about 1/4 in. This redesign proved to be adequate to solve the problem of the substrates surviving the high-acceleration environment.

It did not completely solve the electrical performance problem of the stripline filter — a problem related to proximity effects and resonant cavity responses at the transmitter frequency. The complex problems of the combined performance of the oscillator, frequency multiplier, and

stripline filter indicate a serious reproducibility problem. It is recommended that alternative approaches and materials be evaluated. They should at least include voltage controlled oscillators, other substrate materials, interdigital filters, and other frequency-multiplying techniques.

2. PROGRAM OBJECTIVES

2.1 Scope

The primary objective of this program is to develop an inexpensive, easily reproducible, stable L-band transmitter for telemetering the functional performance of projectiles and to furnish documentation upon which future competitive procurements can be based. The transmitter is to consist of an overtone crystal oscillator, a power amplifier, an SRD frequency multiplier, a filter, and an output amplifier. The multiplier, filter, and output amplifier are to be fabricated in stripline circuitry using metallic conductors on ceramic substrates. The crystal oscillator and power amplifier may be constructed using thick film or printed circuit board techniques. Space and volume efficiency is to be emphasized. Survival at a high-acceleration force equivalent to being fired in the 105-mm howitzer at charge 7 and in the 175-mm gun at zone 3 is required for the completed assembly.

2.2 Specifications

The transmitter specifications (matched into 50 Ω at 25°C unless otherwise noted) are as follows:

Frequency (28 V)		1510.5 MHz ± 0.01%
Power output (24 to 36 V)		100 mW (min.), 300 mW (max.)
Efficiency (ratio of rf output power to dc input power)		10% min. at 28 V
Supply voltage		24 to 36 V dc (current limited to 100 mA)
Frequency stability		± 0.01%
For:	Temperature	-40 to +60°C
	B+	24 to 36 V
	Voltage standing wave ratio	5:1 all phases
	Shock	25 kg, 9 ms
Spurious radiation		40 dB (below the carrier at 28 V)

Modulation type	phase modulation
For modulation index of from 3 to 300 kHz	1.0
Modulation sensitivity	1.0 V max.
Modulation distortion	5% max.
Modulation spectrum (design goal)	3 kHz to 3 MHz
Turn-on frequency stability (at 25°C from 1 ms to 3 min after power turn-on)	± 0.01%
Output impedance	50 Ω
Size	
Diameter (with flat)	1 1/2 in.
Length	1 in.
Output connector	3 mm OSM-220 jack

Components, materials, and subassemblies must be approved by the sponsor before procurement or fabrication. Elements not previously approved for the artillery environment must be submitted for g-testing.

2.3 Documentation

A complete set of drawings prepared in accordance with military standards set forth in HDL TL-PD-37E is to be furnished, along with a final report at the completion of the program. Informal monthly progress reports are to be submitted for the duration of the program.

3. DESIGN DEVELOPMENT

3.1 Specification Review

The program objectives were to correct some performance problems in the Motorola design and to simplify its manufacturability. In reviewing the Motorola L-band transmitter, the following problems in performance were identified by HDL:

(1) The units exhibited unsatisfactory operation over a temperature range of -40 to +65°C.

(2) The oscillator frequency did not stabilize rapidly enough after turn-on.

(3) The units were difficult to manufacture.

In addition to the design changes needed to solve the above problems, HDL requested several other changes from the specifications of the Motorola design:

(1) The supply voltage was to be changed from +13.0 ± 0.5 V to a range of +24 to +36 V.

(2) The usable modulation frequency was to be extended to 3 MHz.

(3) The direct connection of semirigid cable to the transmitter for the output was to be replaced with an OSM-220 jack.

(4) The manufacturability of the transmitter was to be improved while the per unit cost was to be kept between $600 and $1000 in lots of 100.

All other specifications were to remain the same. The complete specification list as it applies to APL* with the above mentioned changes appears in Section 2.2.

3.2 Literature Review of Prior Development Efforts

Several technical reports[1] [2] [3] were reviewed to determine the approaches pursued and the results obtained to provide a starting reference for the APL effort.

3.3 Initial Design Proposal

The basic philosophy as directed by HDL was to modify the Motorola design but to retain their basic approach. Therefore, the APL effort

*"Scope of work: L-band transmitter--APL," 21 October 1975; "Minutes of First Organizational Meeting of HDL L-band Crystal-Controlled Transmitter," JHU/APL EME-75-273 (15 October 1975).

[1]James F. Richardson, "Preliminary Report on the Development of a Crystal Controlled L-Band Artillery Telemetry Transmitter," HDL-TR-1564 (August 1971).

[2]Louis Wunderlich, "Final Report, Crystal Controlled L-Band Telemetry Transmitter," Motorola Contract No. DAAG39-72-C-0074 (September 1973).

[3]F. T. Liss and J. F. Richardson, "Ruggedized Quartz Oscillator Crystals for Gun-Launched Vehicles," HDL-TM-68-23 (July 1968).

started with the Motorola block diagram shown in Figure 1. Several points must be made about this design since the changes and improvements previously mentioned bear directly on them.

(1) The transistors used in the audio amplifier and oscillator circuits have collector-emitter breakdown voltages of 12 V.

(2) The crystal oscillator circuit is heavily coupled into a nonlinear stage, the times-2 multiplier.

(3) The 1.51 GHz interdigital filter is implemented by means of an unbalanced microstrip circuit. This makes its performance susceptible to variations in the potting compound used to encapsulate the transmitter.

(4) The power-amplifier stage lacks temperature compensation.

When these points are compared to the new specification given to APL, the need for modification and redesign of the Motorola transmitter becomes apparent. The higher supply voltage with a 12 V range dictates the incorporation of a voltage regulator. In order to maintain efficiency and not waste too much dc power in regulation, the regulated output voltage should be as high as is practical. Integrated circuit voltage regulators with regulated output voltages of 23 to 24 V are readily available; therefore, regulation to +24 V was selected.

The immediate result of determining the new operating voltage was the need to replace the transistors in the audio-amplifier and oscillator circuits and to redesign the oscillator circuit. The audio amplifier/modulator circuit needed to be redesigned to extend the modulation frequency range upward.

No amount of redesign of the oscillator circuit will improve its turn-on stability when it is loaded with the nonlinearity of the times-2 multiplier stage. The best option here is to add a buffer amplifier between the crystal oscillator and the multiplier.

The approach to the 1.51 GHz filter was at first going to be a balanced stripline interdigital design, as is commonly used. However, after observing the difficulties encountered by Motorola with the interdigital filter, HDL recommended using some other type of filter. A 1/4 wavelength side-coupled filter appeared to be the most likely solution to the filter/size restriction problem. The times-10 SRD circuit would have to be modified to work into the new 1.51 GHz filter.

To correct the rf output power variations with temperature, the power-amplifier stage dc biasing would have to be changed and the rf

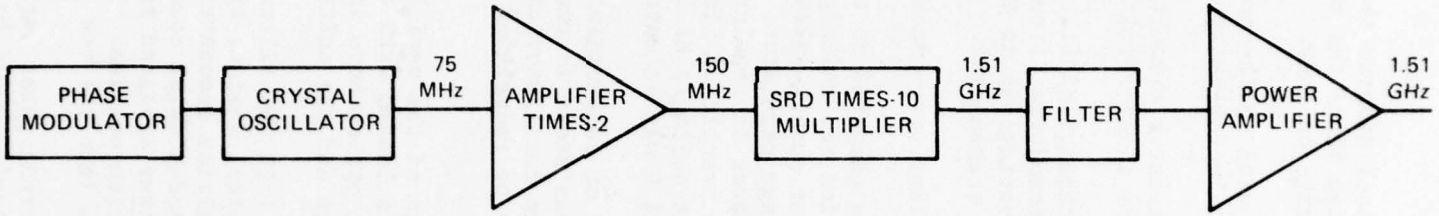


Figure 1. Motorola block diagram of L-band transmitter.

matching modified as needed. There did not appear to be any problem in keeping the same transistor in this stage.

Although the Motorola approach to housing the transmitter was to be retained, a slight mechanical modification was necessary to incorporate the 3 mm OSM jack for the rf output.

3.4 Final Design for Implementation

The final design proposed at the start of the development is shown as a block diagram in Figure 2. The circuit was partitioned by designing three substrates into the housing space containing the following functions:

(1) Board 1: Voltage regulator, oscillator, buffer, and times-2 frequency multiplier

(2) Board 2: Step-recovery diode times-10 frequency multiplier and 1.51 GHz filter

(3) Board 3: Output power amplifier

4. ELECTRICAL DESIGN IMPLEMENTATION

4.1 Modulator, Crystal Oscillator, and 75.5 MHz Buffer Amplifier

The 2N2222A transistor was selected for use in the oscillator and buffer amplifier circuits. It has a collector-emitter breakdown voltage of 40 V and is capable of 19 dB gain at 75.5 MHz. The crystal, which is a fifth-overtone series resonant crystal supplied by HDL, has been specifically packaged to withstand the high-g environment of the L-band transmitter.

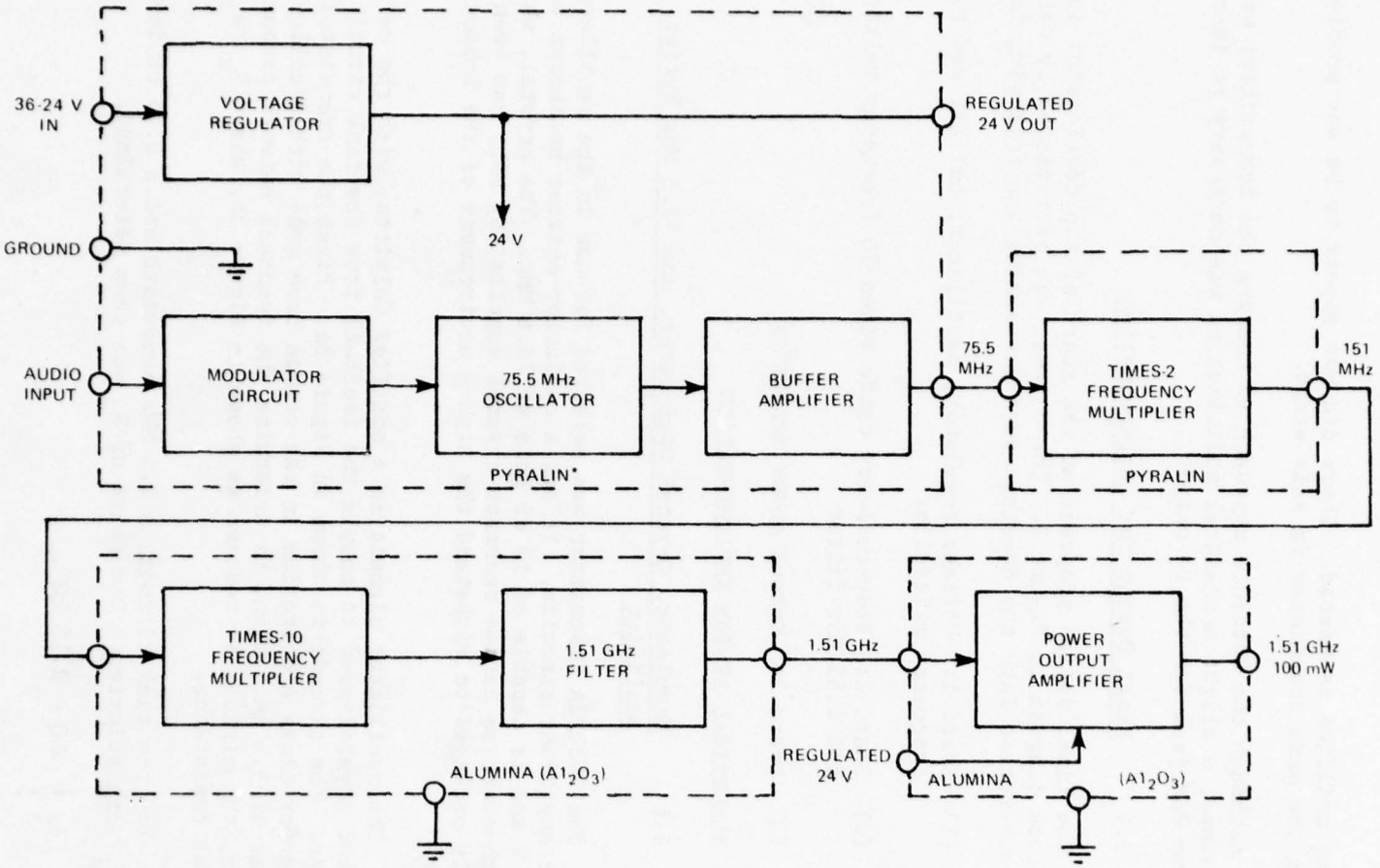
The oscillator circuit is a modified Colpitts, with the series resonant crystal used to couple the feedback from the tank circuit to the emitter. The circuit is shown in Figure 3a. First the transistor is biased for class A operation in the common base mode with a collector current of 3.5 mA. Then, to determine the feedback network component values, the circuit is redrawn as shown in Figure 3b, where R_x is the crystal resistance.

For the tank circuit, a 2.5 MHz bandwidth and a 0.15 μH inductor for L_1 were selected. The value of R_2 was then determined.

$$R_2 = \omega LQ = 2.13 \text{ k}\Omega ,$$

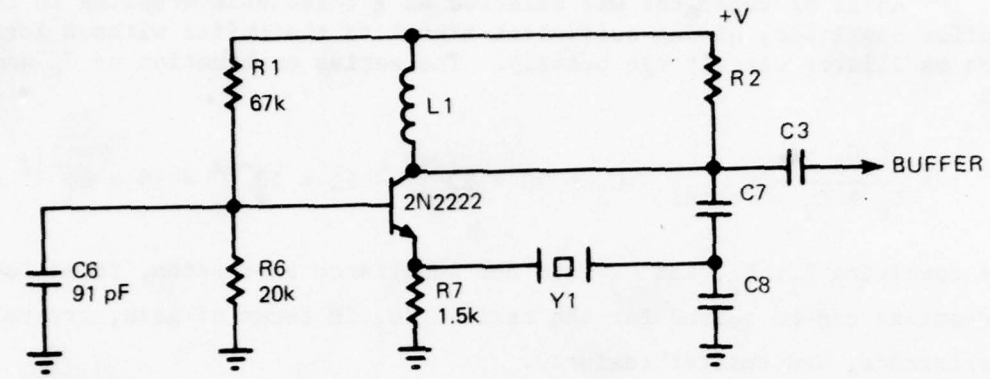
where

$$Q = \frac{75.5 \text{ MHz}}{2.5 \text{ MHz}} = 30.2 .$$

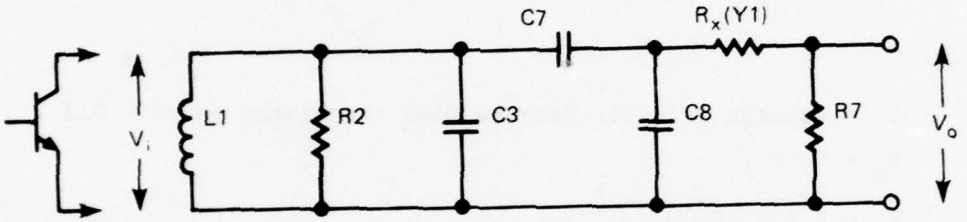


* A DuPont trade mark for their polyimide material.

Figure 2. APL block diagram of L-band transmitter.



(a)



(b)

Figure 3. Modified Colpitts oscillator circuit.

The total capacitance needed to resonate this circuit is

$$C_{total} = \frac{Q^2 L_1}{R_2^2} = \frac{(30)^2 (0.15 \times 10^{-6})}{(2.1 \times 10^3)^2} = 3.0 \times 10^{-11} ,$$

where

$$C_{total} = \frac{C_8 C_7}{C_8 + C_7} + C_3 .$$

An 11 pF capacitor was selected as a reasonable coupling to the buffer amplifier, giving sufficient signal to the buffer without loading the oscillator circuit too heavily. The series combination of C_8 and C_7 is

$$\frac{C_8C_7}{C_8 + C_7} = C_{total} - C_3 = 30 \times 10^{-12} - 11 \times 10^{-12} = 19 \times 10^{-12} .$$

By combining L_1, R_2, and C_3 into one admittance expression, three loop equations can be solved for the ratio C_8/C_7 in terms of gain, crystal resistance, and emitter resistor.

$$\frac{C_8}{C_7} = \frac{\frac{R_7}{G} - (R_x + R_7)}{R_x + R_7} ,$$

where

G = voltage gain for network plus transistor gain* = 0.2 ,

$R_x = 50\ \Omega$,

$R_7 = 1.5 \times 10^3\ \Omega$,

and

$$\frac{C_8}{C_7} = \frac{\frac{1.5 \times 10^3}{0.2} - (50 + 1.5 \times 10^3)}{50 + (1.5 \times 10^3)} = 3.83 .$$

Then, to find C_8 and C_7,

$$C_8 = 3.83C_7 ,$$

$$C_7 = \frac{\frac{C_8C_7}{C_8 + C_7}(3.83 + 1)}{3.83} = \frac{19.0 \times 10^{-12}(3.83 + 1)}{3.83} = 24.0 \times 10^{-12} ,$$

$$C_8 = 3.83(24.0 \times 10^{-12}) = 91.8 \times 10^{-12} .$$

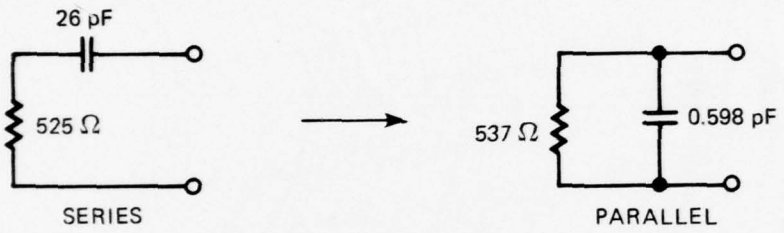
*G cannot be less than 0.

Optimization of the engineering model of the oscillator circuit determined the best values to be C_7 = 30 pF, C_8 = 91 pF, and R_2 = 2.7 kΩ. The frequency was 75.524 MHz when operating into the buffer amplifier.

The 75.5 MHz buffer amplifier is biased for class A operation with a collector current of 3.5 mA. In order to determine the collector circuit values, the output impedance was measured at 75.5 MHz. This series impedance was then converted to the equivalent parallel impedance and plotted on a Smith Chart.

$$\rho_{out} = 0.827 \angle -1.6° \rightarrow Z_{out} = (10.5 - j1.6)50$$

$$Z_{out} = 525 - j80 \ .$$

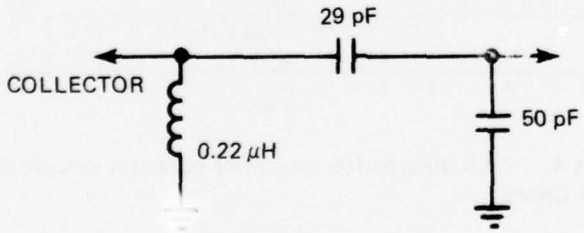


where

$$R_p = R_s\left[1 + \left(\frac{X_s}{R_s}\right)^2\right] = 525\left[1 + \left(\frac{80}{525}\right)^2\right] = 537 \ ,$$

$$X_p = \frac{R_p}{X_s/R_s} = \frac{537}{80/525} = -j(3.52 \times 10^3) \ .$$

Using the Smith Chart (Figure 4), the following collector circuit was derived:



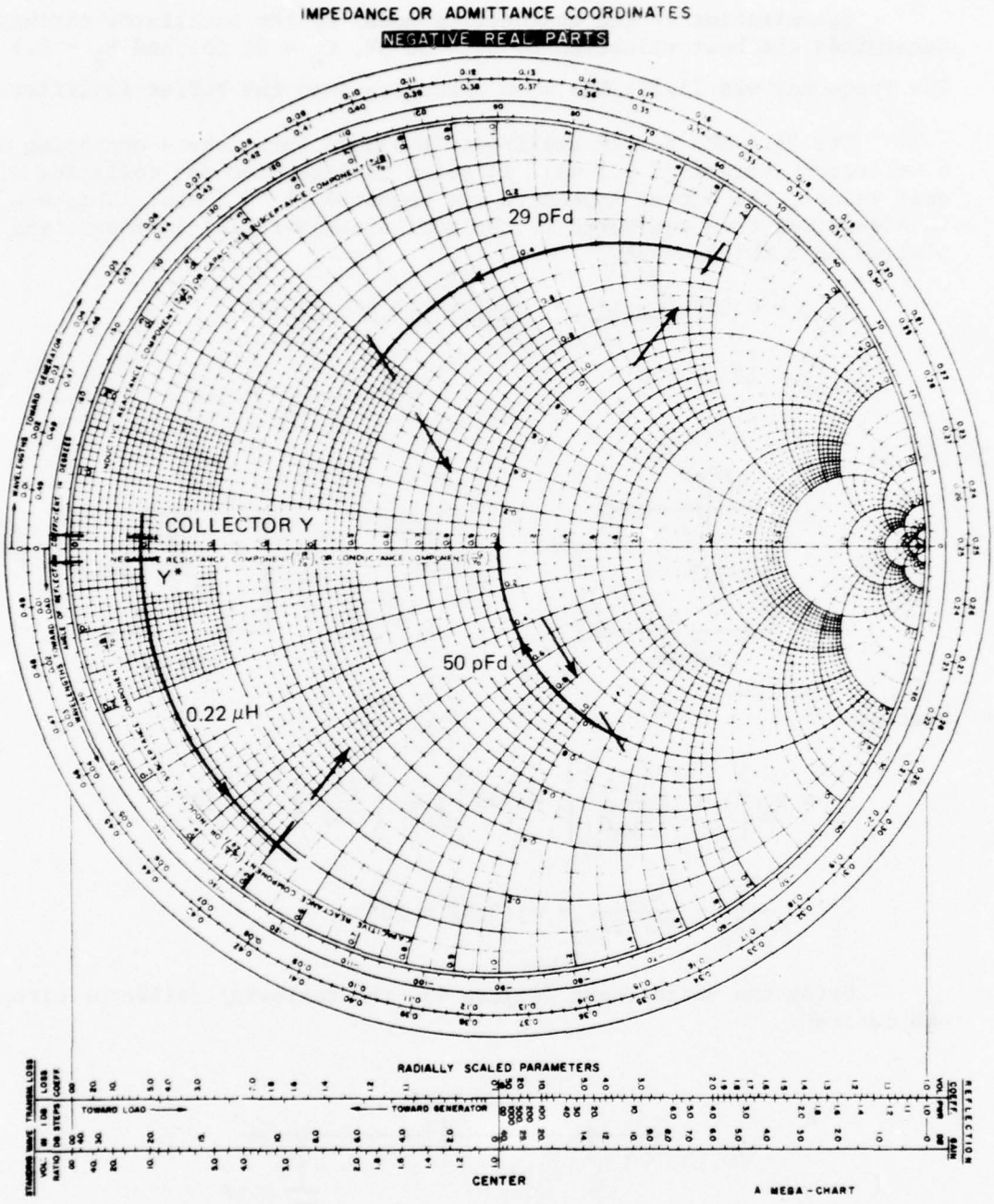
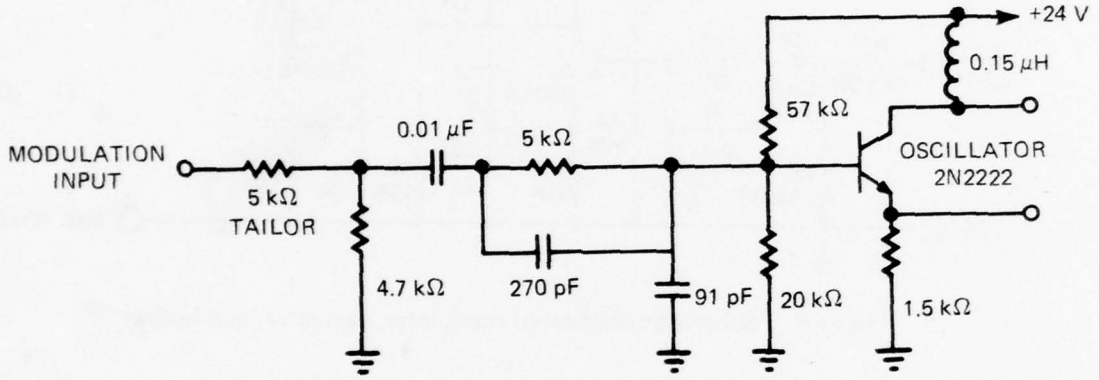


Figure 4. 75.5 MHz buffer amplifier collector circuit derivation Smith Chart.

The input to the 75.5 MHz buffer was lightly coupled to the oscillator with an 11 pF capacitor to minimize the load effect on the oscillator. Modulation is accomplished by phase-modulating the oscillator. The modulation signal is coupled to the base of the transistor in the oscillator circuit by a frequency-compensating RC network. The base bypass capacitor has been made as small as is practical while still maintaining the necessary gain in the transistor to reduce its effect on the modulation signal. The primary modulation frequency range of 3 to 300 kHz has been met and the upper limit extended to 750 kHz. Above this frequency, AM modulation distortion becomes apparent. The design goal for extending the upper frequency of the modulation signal, acceptable by the modulation circuit, was 3 MHz.



The 5 kΩ resistor at the modulation input is used to tailor the deviation 0.05 radian at 75.5 MHz for a 1.0 V signal level.

The oscillator, buffer, modulator circuit, and voltage regulator are assembled on one board (referred to as board 1). Originally, this board had included the times-2 multiplier stage, but the extreme closeness of the parts caused spurious oscillations, and the times-2 multiplier was put on an additional board. The schematic diagram of this circuit on board 1 is shown in Figure 5. Figure 6 is a photograph of board 1, the original design with all the parts in place.

4.2 Times-2 Frequency Multiplier

The 75.5 to 151 MHz (times-2) multiplier stage must not only double the signal frequency but must also provide a 12 dB gain in order to supply a 100 to 125 mW signal level to the times-10 multiplier. The transistor (KD4025) that was selected had a gain bandwidth product of 1.0 GHz and an

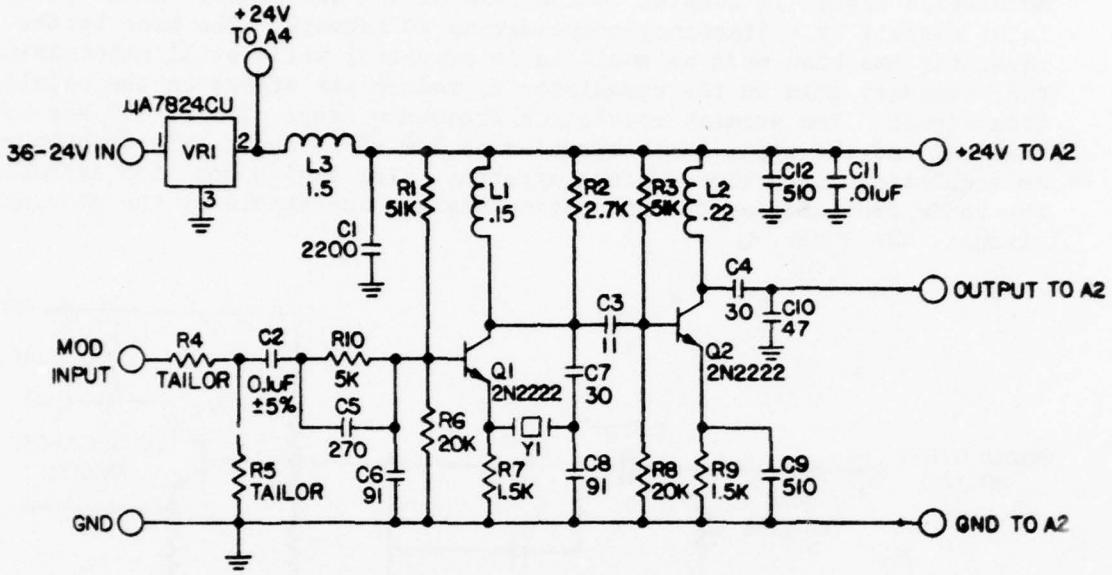


Figure 5. Schematic diagram of modulator, oscillator, and buffer.

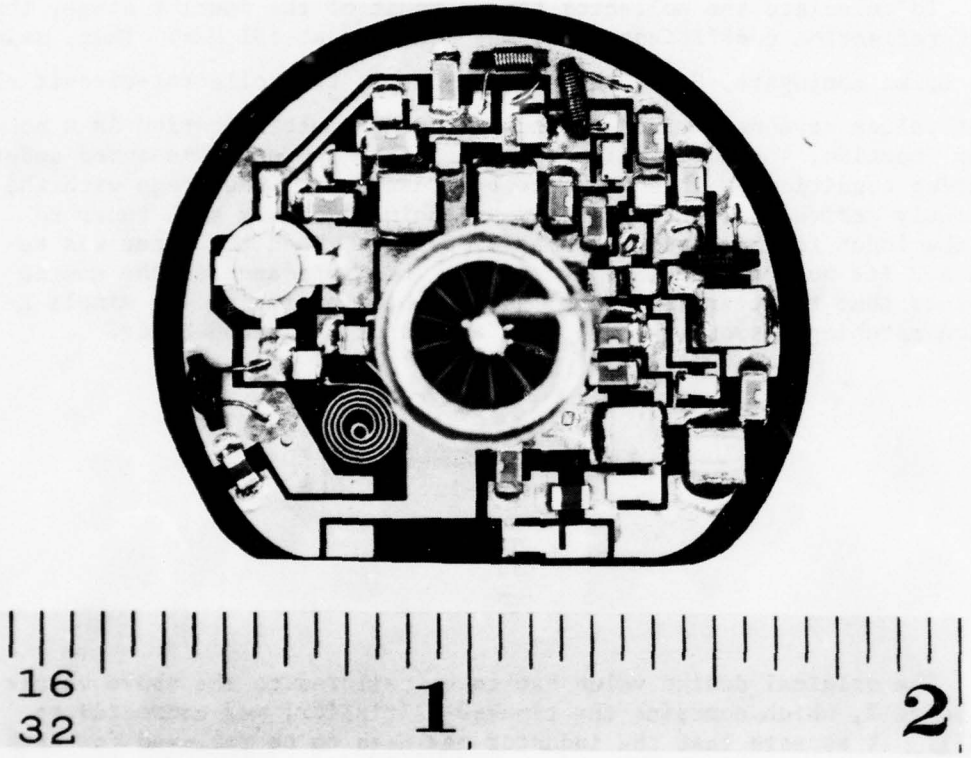
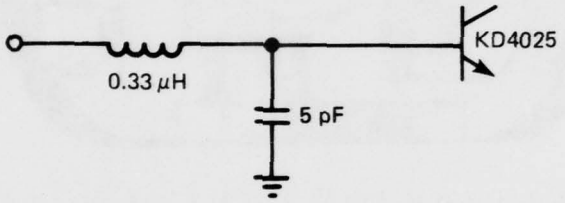


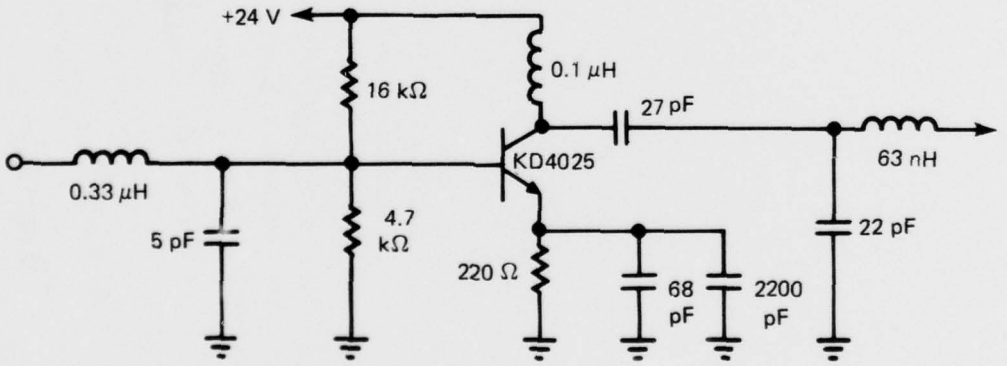
Figure 6. Original design for board 1 with parts in place.

emitter-collector breakdown voltage, V_{CEO}, of 25 V. This device also has the advantage of being available in a ceramic microstrip package.

To calculate the collector tank circuit of the doubler stage, the output reflection coefficient, S_{22}, was measured at 151 MHz. Then, using the complex conjugate, S_{22}^*, and a Smith Chart, the collector-circuit component values were determined. Since frequency multiplication is a nonlinear function, the input reflection coefficient must be measured under operating conditions. This was done by constructing the stage with the previously derived collector circuit and using a double stub tuner to tune the input for best operation as a doubler. Then the tuner was removed and its output impedance measured. This impedance is the source impedance that the transistor must see for best operation. A simple L-section matching network was used for the input, as shown below.



The original design value had to be tailored to the above values when board 2, which contains the times-2 multiplier, was connected to board 1. It appears that the inductor may need to be tailored for each pair of connected boards. The completed circuit schematic is shown below.



4.3 Times-10 Multiplier and 1.51 GHz Filter

The times-10 multiplier circuit contains an input matching network, a bias circuit, an impulse generator, an SRD, and output resonators. The SRD selected was the Hewlett-Packard 5082-0314, which is an HP 5082-0360 chip mounted in a leadless inverted device (LID) package.

The component values for the circuit were based on information contained in a Hewlett-Packard Application Note[4] and were determined as follows:

Impulse generator

$$\text{Inductor } L_D \simeq \frac{t_p^2 - t_t^2}{\pi^2 C_{VR}} = \frac{(4.96 \times 10^{-10})^2 - (360 \times 10^{-12})^2}{\pi^2 (4.18 \times 10^{-12})}$$

$$= 2.83 \times 10^{-9} \text{ H} .$$

$$\text{Capacitor } C_T \simeq \frac{C_{VR}}{(2 f_{in} t_p)^2} = \frac{4.18 \times 10^{-12}}{[2(1.51 \times 10^{8})(4.96 \times 10^{-10})]^2}$$

$$= 1.86 \times 10^{-10} \text{ F} ,$$

where

$t_t = 360 \times 10^{-12}$ s ,

$\tau = 312 \times 10^{-9}$ s ,

$C_{VR} = 4.18 \times 10^{-12}$ F , and

$t_p = 4.96 \times 10^{-10}$ s .

---

[4]"Harmonic Generation Using Step Recovery Diodes and SRD Modules," Hewlett-Packard Application Note 920, Hewlett-Packard Co., Palo Alto, CA 94304.

Matching Network

$$R_{in} = \frac{\omega L_D}{2(\cos \alpha) \sin (\alpha - \frac{\pi}{n})}$$

$$= \frac{2\pi(1.51 \times 10^8)\ (2.83 \times 10^{-9})}{2(\cos 49°) \sin (49 - \frac{180}{10})}$$

$$= 3.95\ \Omega\ .$$

$$\text{Inductor}\quad L_M = \frac{1}{\omega}\sqrt{R_{in}(R_g - R_{in})}$$

$$= \frac{1}{2\pi(1.51 \times 10^8)}\sqrt{3.95(50 - 3.95)}$$

$$= 14.2 \times 10^{-9}\ \text{H}\ .$$

$$\text{Capacitor}\ C_M = \frac{1}{\omega R_g \sqrt{\frac{R_{in}}{R_g - R_{in}}}}$$

$$= \frac{1}{2\pi(1.51 \times 10^8)(50)\sqrt{\frac{3.95}{50 - 3.95}}}$$

$$= 71.8 \times 10^{-12}\ \text{F}\ ,$$

where

α = conduction angle of 49° ,

R_g = 50 Ω , and

n = multiplier number .

Bias Circuit

$$R_b = \frac{5\tau}{n^2 C_{VR}}$$

$$= \frac{5(312 \times 10^{-9})}{10^2(4.18 \times 10^{-12})}$$

$$= 3.73 \times 10^3\ \Omega\ .$$

The 1.51 GHz filter is used to attenuate the unwanted harmonics in the output of the times-10 multiplier. The first design was an interdigital filter using three 1/4 wavelength resonators grounded at one end. This design offered compact physical size and sharp roll-off of frequencies below the bandpass.

HDL informed APL that Motorola had used this filter design with microstrip construction and had difficulty in reproducing it. It was HDL's opinion that the problem arose from the difficulty of manufacturing the ground connections for the 1/4 wavelength resonator and from the effect of the potting on the filter circuit. The use of a balanced stripline design to construct the filter was recommended by HDL to eliminate having to ground the resonators.

To satisfy these requirements, a parallel coupled filter was designed using the procedure of Matthaeu, Young, and Jones.[5] It is a three-pole filter with a Tchebysheff response having a 5 percent bandwidth and 50 Ω impedance. The resonators are 1/2 wavelength long, with coupling between adjacent 1/4 wavelength sections, as shown in Figure 7. Thus, the need for gounding has been eliminated. The use of balanced stripline construction has removed the potting from direct contact with the filter, thereby eliminating its effect.

The filter does create a packaging problem: how to fit a filter whose total length is 2.47 in. onto a substrate 1 1/4 in. in diameter. The solution was to design the filter in a curved path around the perimeter of the substrate close to the edge, allowing sufficient space in the

[5]George L. Matthaei, Leo Young, and E. M. T. Jones, Microwave Filters, Impedance Matching Networks, and Coupling Structures, McGraw Hill, New York (1964), page 473.

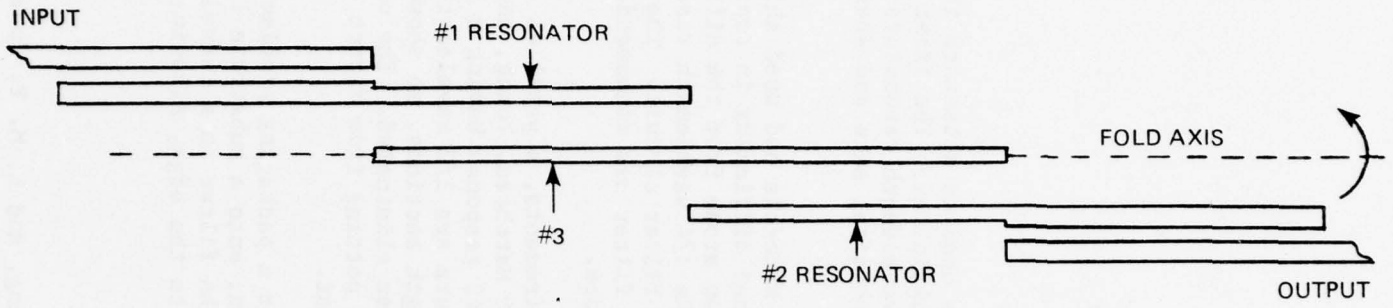


Figure 7. Parallel coupled filter design (Matthaei, Young, and Jones, Microwave Filters, Impedance-Matching Networks, and Coupling Structures, McGraw-Hill, New York, 1964).

center area for the times-10 multiplier circuit. This was accomplished by folding the stripline filter about the resonator, symmetrically about the axis, as is shown in Figure 7. The resulting geometry of the filter on the substrate is shown in Figure 8.

To evaluate the filter design, an engineering model was first etched on an Epsilam-10 (a product of the 3M Co.) substrate. Testing showed that deforming the filter by curving and folding degraded its performance. The bandwidth was wide because the resonators were off frequency, and the roll-off outside the bandpass was too slow. To correct these problems, the filter was tailored. The space between resonator #2 and those adjacent to it was decreased (Figure 8). The ends 'a' of resonators #1 and #3 were trimmed to prevent coupling between them. After this tailoring, the performance of the filter was satisfactory and the following parameters were measured:

Insertion loss	2.9 dB ,
Bandwidth	85 MHz ,
Center frequency	1.52 GHz .

The next step in the design was to combine the times-10 multiplier circuit and the 1.51 GHz filter on an alumina substrate. The problems found with the filter were a 20 dB notch on the high-frequency side of the bandpass and a 12 dB insertion loss at 1.51 GHz. The notch was caused by coupling between the filter and the 1.51 GHz resonators in the times-10 multiplier that are close to the filter on the substrate. The times-10 resonators were shorted to ground so that the filter could be evaluated. This eliminated the notch and 6 dB of the insertion loss. The bandpass, now 90 MHz high, was caused by a thin air gap between the alumina substrate and the alumina dielectric cover. This gap was filled with Delta Bond 152 (a product of Wakefield Engineering Co.), which acted as a filler between the two pieces of alumina as well as a bond. The performance of the filter was improved but remained unsatisfactory. The measured parameters were as follows:

Insertion loss	6 dB ,
Outer frequency	1.507 GHz ,
Impedance	26 + j30 Ω ,
Bandwidth	60 MHz .

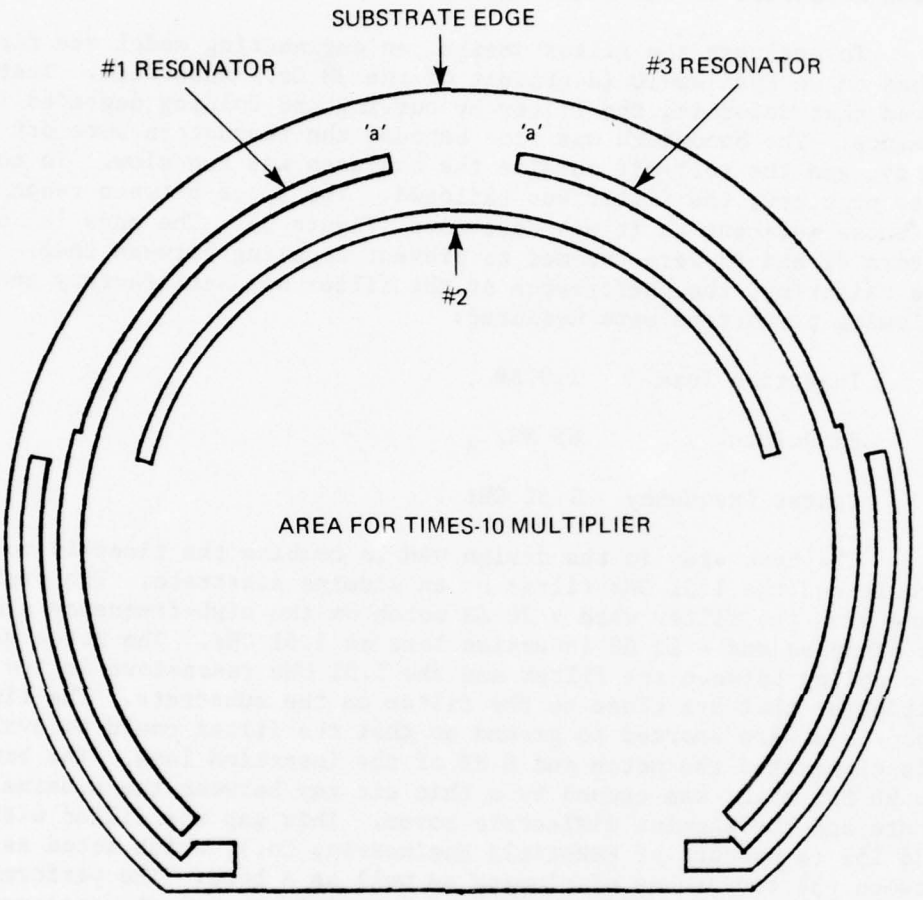


Figure 8. Folded parallel coupled filter.

The times-10 multiplier would not function properly when loaded with the 26 Ω input impedance of the filter; attempts to modify the multiplier to work with the filter were unsuccessful. How much of this problem was due to the coupling between the resonator in the multiplier and the 1.51 GHz filter could not be determined. The limited packaging volume did not allow greater separation of the two circuits. Figure 9 is the schematic diagram of the times-10 frequency multiplier and the 1.51 GHz filter.

4.4 1.51 GHz Power Amplifier

The power amplifier is required to provide a 10 dB gain with a 100 mW output, to operate into a high voltage standing wave ratio (VSWR) without failing, and to maintain the output power over the temperature range. The transistor used for this amplifier is HP35831E, which is selected by the manufacturer for a minimum gain of 10 dB at 1.51 GHz. The amplifier is operated as class B to avoid the difficulty of providing emitter bypassing and to provide temperature compensation by means of a diode in the base bias circuit.

To design the input matching and collector circuits of this nonlinear amplifier stage, the transistor was operated in a test fixture with the desired bias and stub tuners on the input and output. The tuners were adjusted for best operation and for stable, failure-free operation into a high VSWR. The data thus obtained were plotted on Smith Charts, and the components and transmission lines necessary to match the amplifier were determined.

Figure 10 is the Smith Chart used to determine the input circuit for the amplifier. The input was originally matched to 50 Ω; however, it has been changed to match to 26 Ω so that the 1.51 GHz filter (with an output impedance of 26 Ω) on the alumina substrate could be used. The efficiency of the amplifier was compromised in order to guarantee safe and stable operation into a high VSWR. This was done by lowering the collector load below optimum and heavily loading the collector. The determination of the collector/output circuit is shown on the Smith Chart (Figure 11). Figure 12 is the schematic diagram of the power output amplifier.

4.5 Interrelation of Circuit Board Position, Interconnections, and Material Strength

When the four circuit boards were assembled into the transmitter housing, consideration had to be given to the problems of interconnections, grounding, rf coupling, and the strength of the alumina substrates. The A1 and A2 boards (modulator, oscillator, buffer, and times-2 multiplier) are bonded back-to-back and the +24 V supply voltage and rf signal

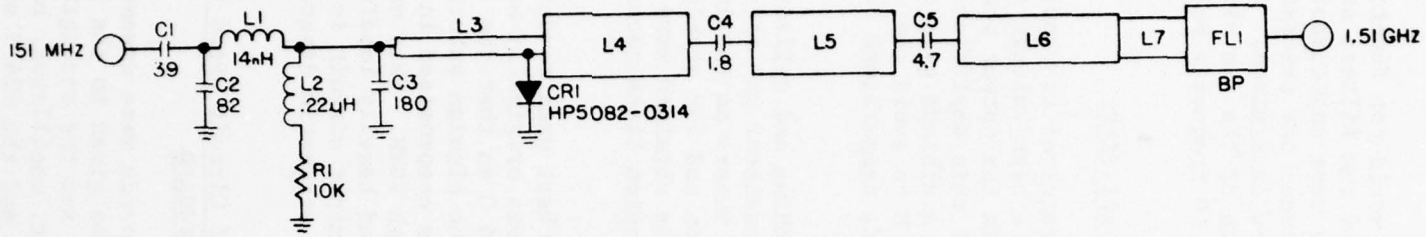


Figure 9. Schematic diagram of times-10 frequency multiplier and filter.

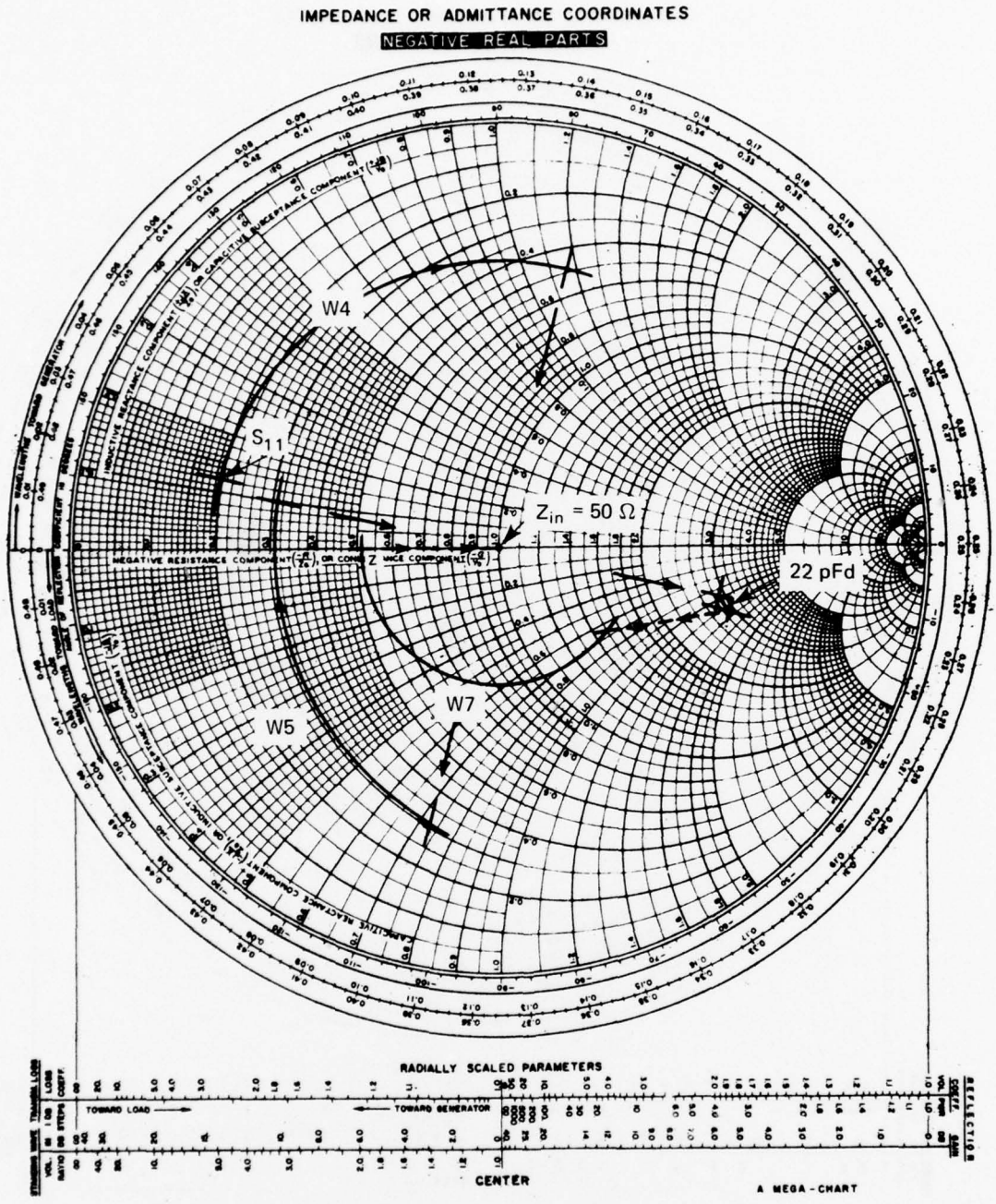


Figure 10. 1.51 GHz power amplifier input circuit determination Smith Chart.

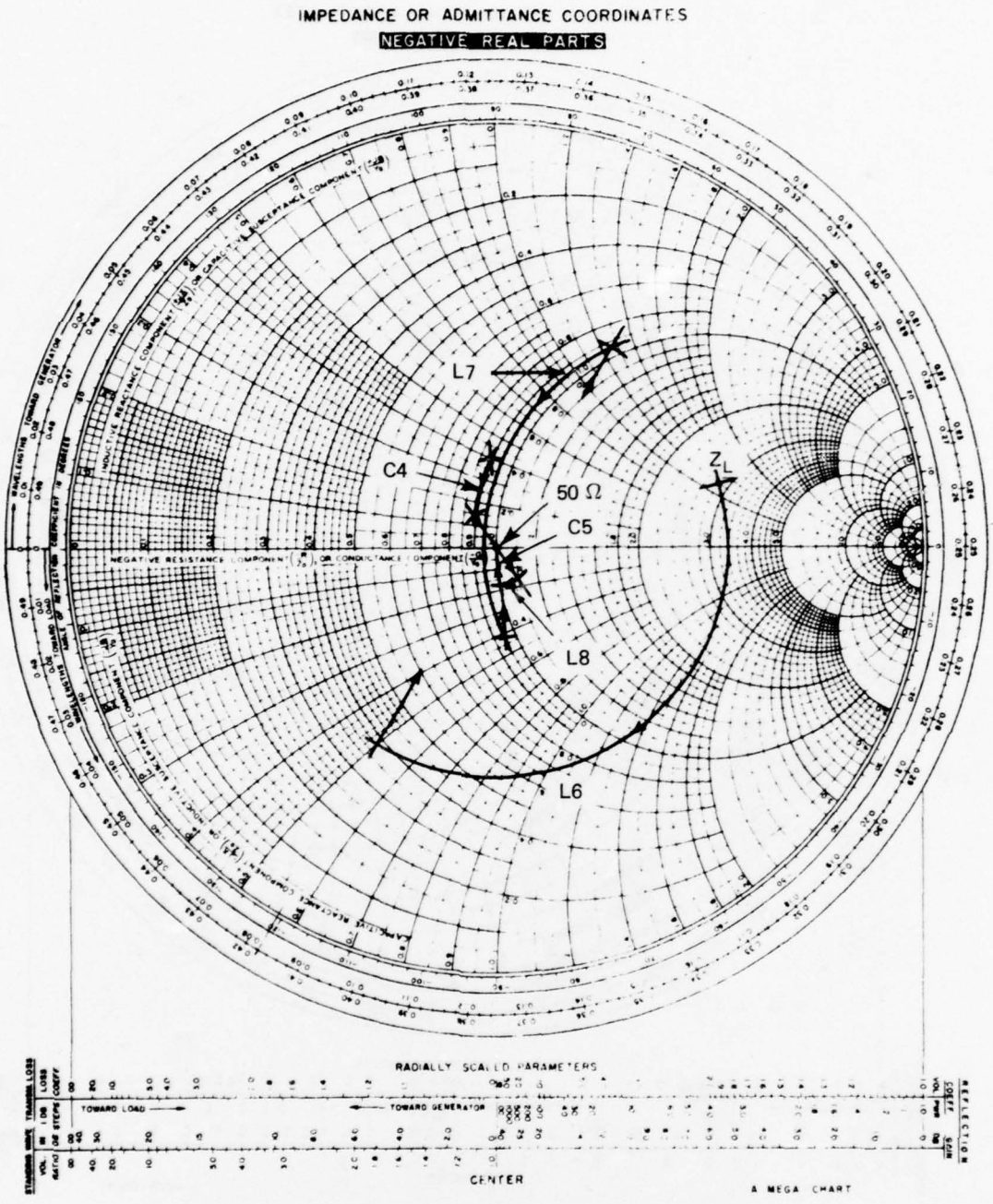


Figure 11. 1.51 GHz power amplifier output circuit determination Smith Chart.

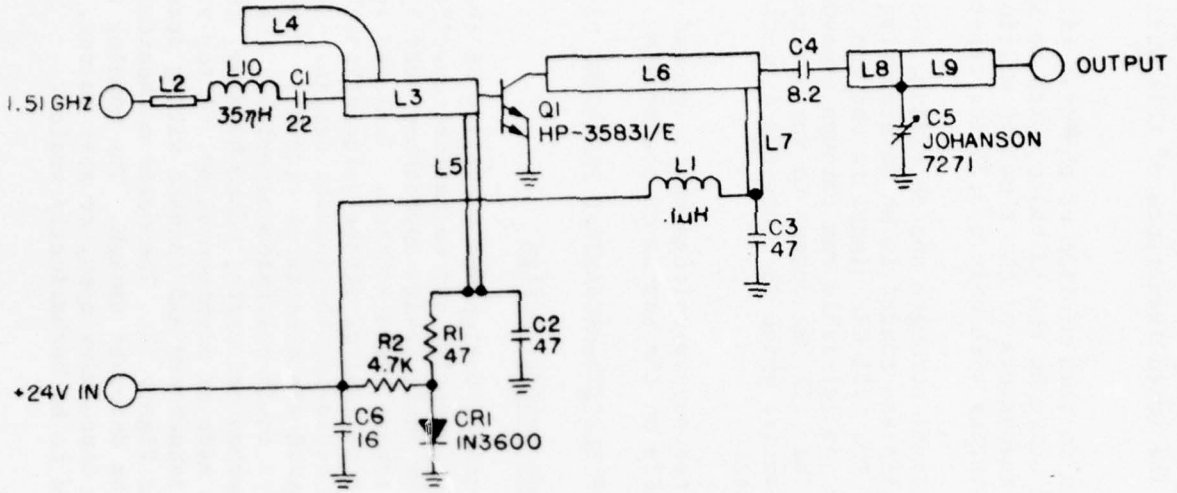


Figure 12. Schematic diagram of power output amplifier.

can be connected by simple wiring through the two boards. The rf signal is carried between the A1/A2 board combination and the A3 (times-10 multiplier and filter) board by standard AWG 26 wire. Coaxial cable could not be used because the assembly procedure prohibits grounding of the coaxial cable shield. The added inductance of this wire could cause an rf mismatch.

One other concern in this section of the transmitter assembly is the proximity of the A2 board to the A3 board, with no shielding between them. This leaves the resonators of the times-10 multiplier facing the times-2 transistor multiplier with only a 0.25 in. separation.

To provide mechanical strength and shielding, the A3 board and the power amplifier board (A4) are bonded in an interhousing with a 0.1 in. floor separating them. The 1.51 GHz signal is coupled from the A3 to the A4 board using RG178B/U coaxial cable run through grooves provided for it in the inner housing. The 1.51 GHz output to the antenna is brought out through an OSM 220 connector, which is connected directly to a pad on the power amplifier substrate.

The +24 V regulated supply voltage and dc ground are carried on wires run through channels on the inside of the housing.

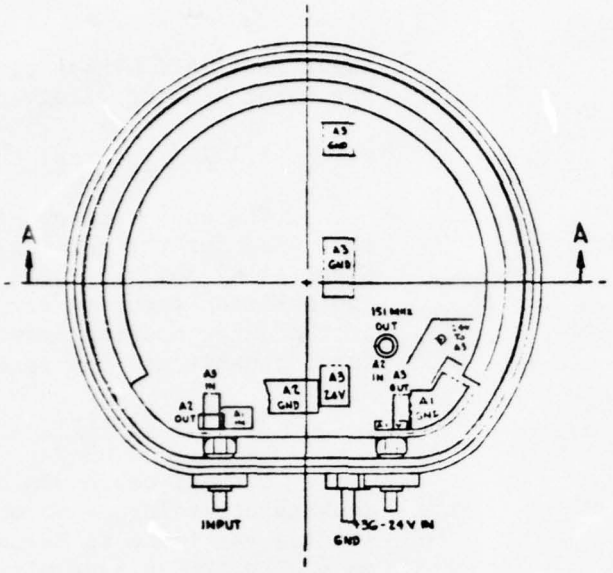
5. IMPLEMENTATION OF ELECTRO-MECHANICAL PACKAGING DESIGN

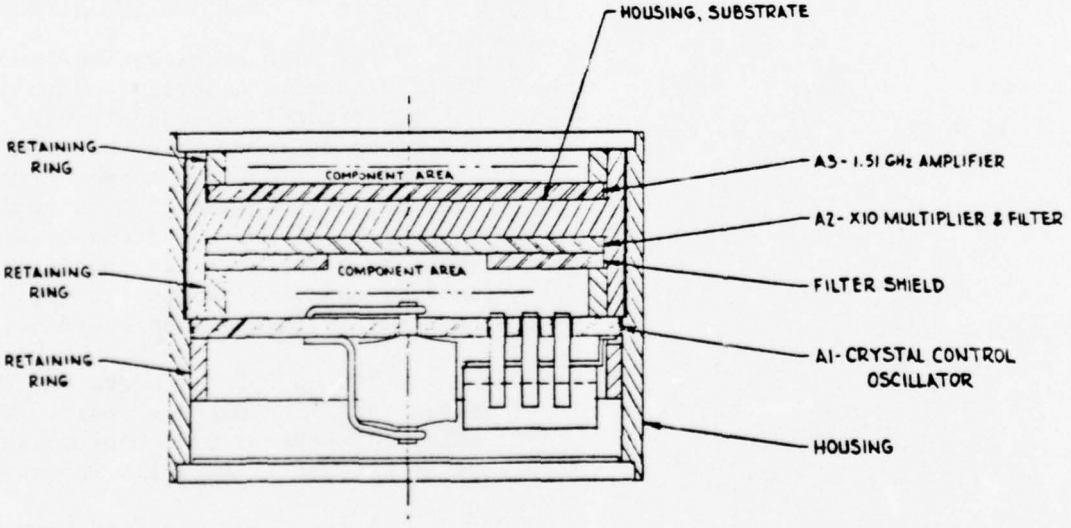
5.1 Initial Mechanical Design

The initial mechanical design and packaging of the L-band transmitter was based on circuit-design and mechanical-specification requirements. Also, some of the basic design approaches used by Motorola (described in their final report) were adopted. Included in Appendix 2 of the Motorola report is a mechanical stress calculation that helped to shorten APL's effort in achieving the initial design. Three hybrid substrate assemblies contained the electrical circuit. One was of Pyralin (a Du Pont trade name for their polyimide material); the other two were alumina ceramic. The mechanical parts, outer housing, inner chassis, and two end-plate caps were made of aluminum alloy. A top view, a cross-sectional view, and an interboard and chassis wiring drawing of this initial design are shown in Figure 13. The outer mechanical dimensions remained unchanged from the Motorola design. The housing end plates could be attached with either conductive epoxy or soft solder. The final enclosure was not required to be hermetically sealed.

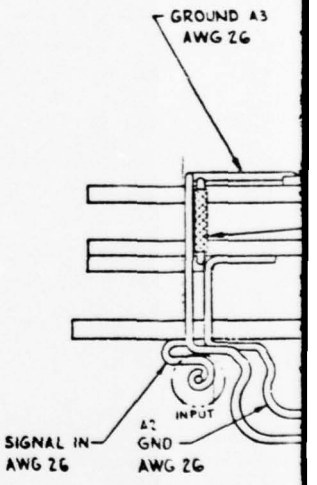
5.1.1 Housing

The material selected for the housing was aluminum alloy 7065 rod, QQ-A-225/9 temper. The top and bottom covers were aluminum alloy 7065



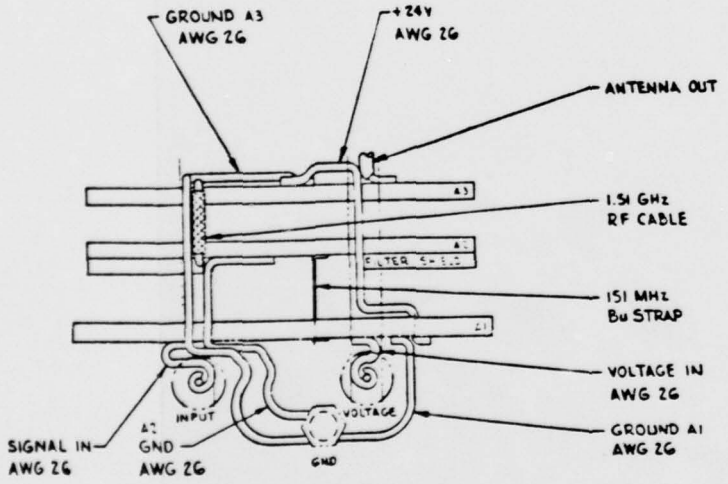


SECTION A-A



INTERBOARD &
WIRI

Figure 13. L-band transm



INTERBOARD & CHASSIS
WIRING

Figure 13. L-band transmitter assembly drawing, initial design.

sheet material. These parts were produced initially by manual machining. The first housing received no additional surface finishing treatment.

5.1.2 Internal Chassis

The substrate housing (internal chassis) material was the same as that used for the housing. Internal retaining rings made of stainless steel alloy 301 were used in three locations to maintain proper spacing and position security for the substrates. Shoulder steps on the inside of the outer housing provided the position reference for locating this inner chassis and the retainer rings.

5.1.3 Electrical Interconnections

Coaxial cable was considered for the electrical connections between substrate levels. However, only one coaxial cable connection between substrates was found to be necessary. All other such interconnections were made with AWG 26 buss wire. The antenna output was to be terminated directly into a semirigid antenna wire. A modulator input resistor-divider mounted externally to the housing was provided for by adding an insulated feedthrough in addition to the two used for power and modulation-signal input.

5.1.4 Potting and Closure

The high acceleration forces required that all internal air spaces be eliminated. A potting compound was proposed. The high-frequency signal performance depends strongly on the dielectric constant and loss factor of materials within the electric field of the circuits. These properties of the potting compound are also very important. The material selected was Stycast 35DS, a product of Emerson & Cuming. It is a polystyrene-based thermosetting casting resin and contains silica microballoons as a filler. Its specific gravity is 0.7, dielectric constant, 1.7 to 1.9, and dissipation factor, 0.004. The material will cure at room temperature in about 48 hours or at 65°C in 16 hours.

The end-plate covers can be attached with either soft solder or electrically conductive epoxy. The recommended materials are indium-tin alloy (40 percent indium by weight) or Ablebond 36-2, a silver-filled epoxy product of Ablestik Laboratories.

5.2 Gunfire Test Results

Figure 13 (the initial design) shows the assembly of the circuit boards in view A-A. The A2 and A3 boards are alumina ceramic and are subject to the fracture if flexed beyond a safe limit during gunfire.

The first gunfire tests were conducted on this design at an acceleration of 42 kg. Figure 14 shows photographs of the A2 and A3 boards after the test. The radial fracture cracks were the result of flexing of the metal web between the two ceramic boards. Calculations indicated that with a web thickness of 0.047 in. the flexing reached a maximum of 0.0617 in. displacement. In order to reduce the flexing to an acceptable level, the web thickness should be at least 0.087 in. thick.

5.3 Redesign and Test

The design was reviewed and a solution was proposed to increase the housing length by 0.175 in. to a final length of 1.275 in. However, additional consideration was given to relieving the overcrowding of electrical parts on board 1 by adding one more substrate to repartition the circuitry ahead of the times-10 frequency multiplier. This added length also provided the necessary space for mounting an OSM 220 connector for the output signal, to replace the semirigid antenna wire in the original design. The inside terminal of the OSM 220 connector terminated directly at the output circuit pad on board 4, the power amplifier output.

5.4 Final Mechanical Design

The details of the final design are shown in Figure 15. The identification of the circuit boards was changed to the following:

Board No.	Description	Material
A1	Crystal oscillator	Pyralin
A2	Times-2 multiplier	Pyralin
A3	Times-10 multiplier and filter	Alumina
A4	1.51 GHz amplifier	Alumina

A computer program was developed to produce the housing on a Bridgeport II numerically controlled machine. The materials in the final housing design were not changed. Details are shown in Figure 16. The parts made of aluminum alloy 7065 were electroplated with gold over electroplated copper over electroless nickel to provide a more lasting corrosion-free surface. A slight radius was ground on the corners of alumina boards 3 and 4 to provide proper fit into the housing. With the design changes, the ceramic substrates survived the gunfire test.

The detailed documentation for reproducing the transmitter hardware, along with the complete data package, has been furnished to Harry Diamond Laboratories.

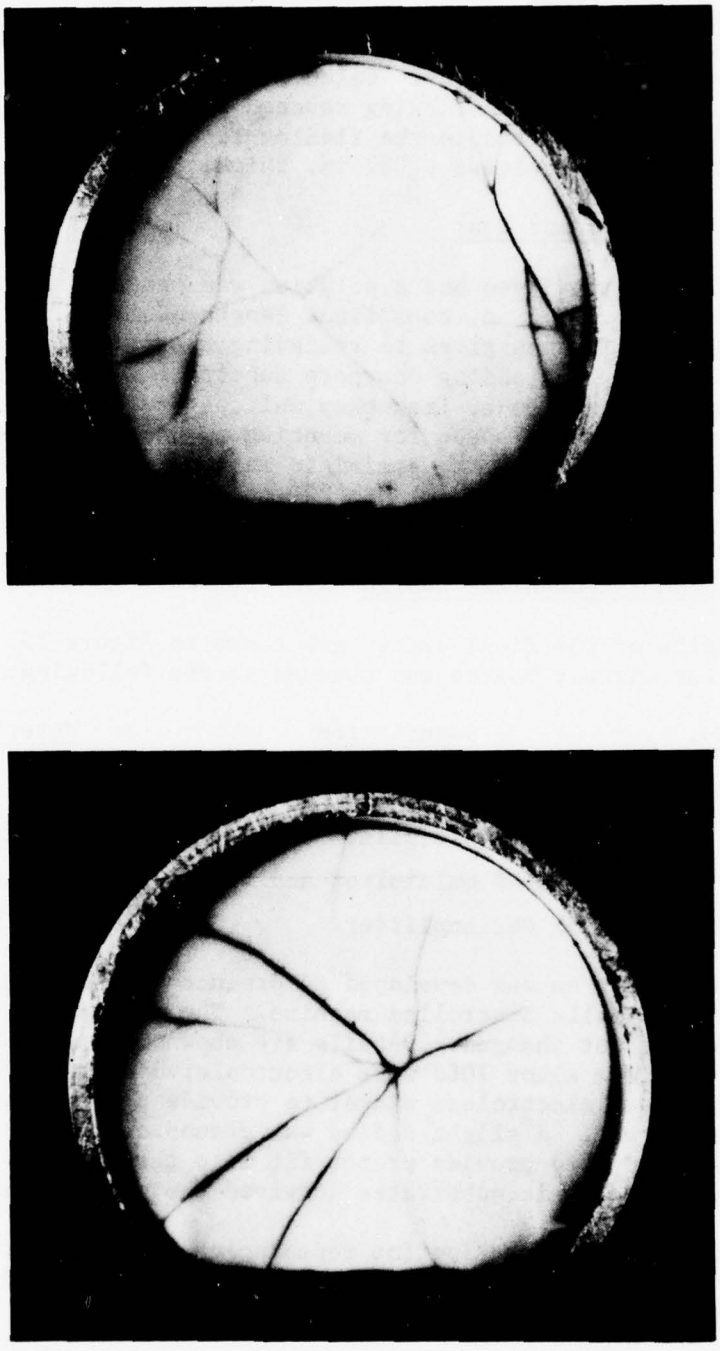
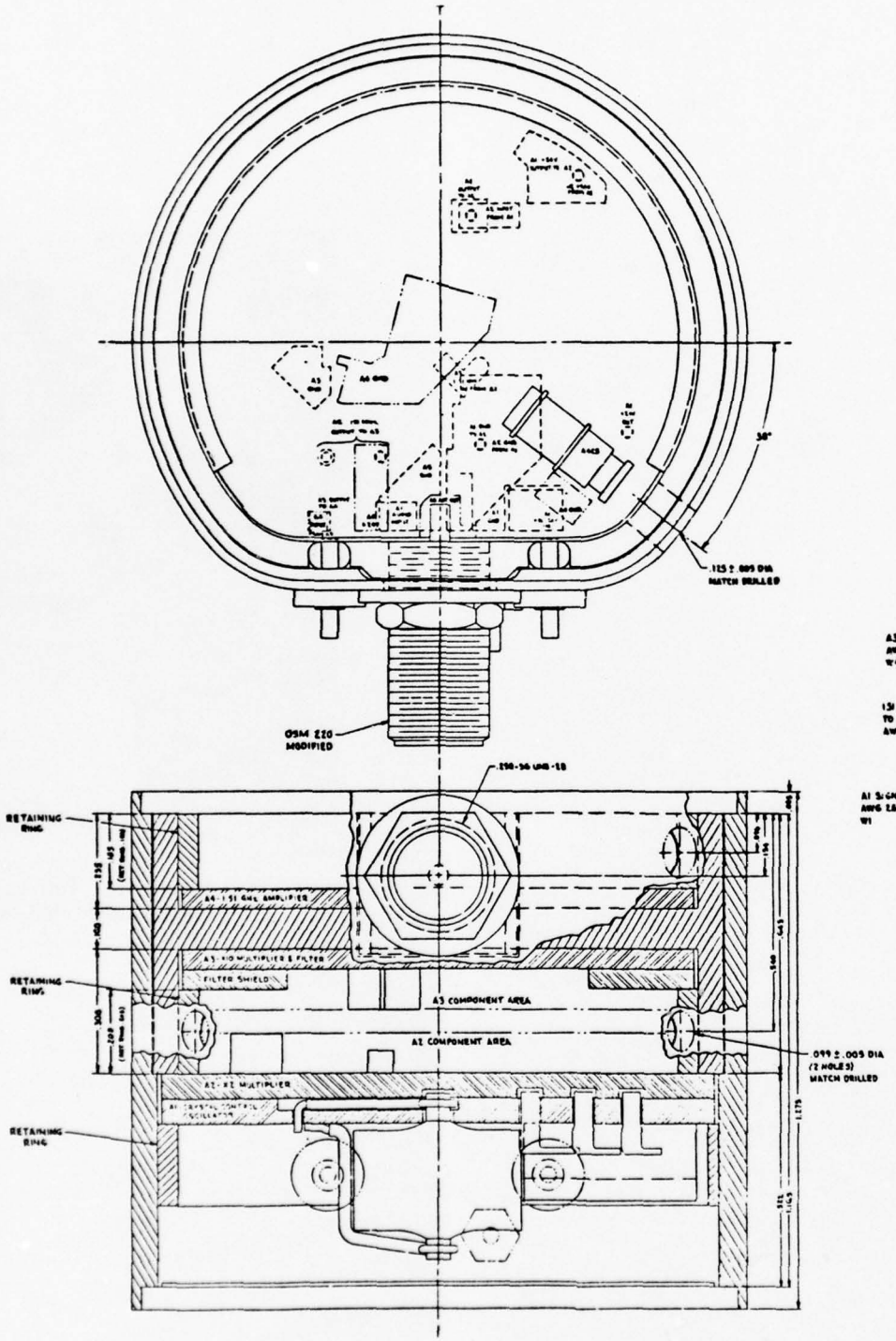
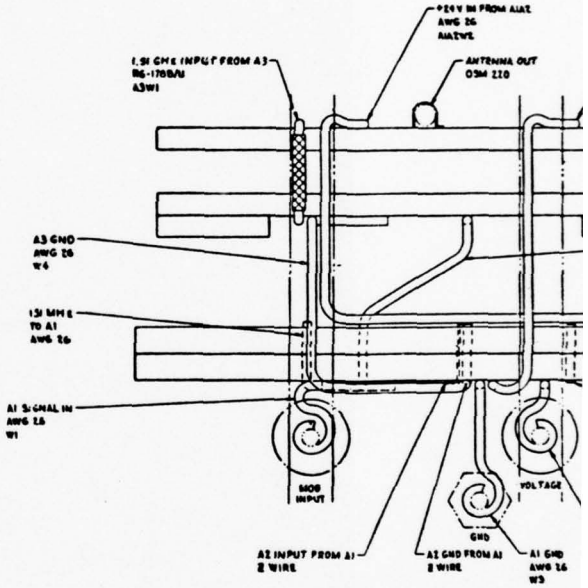


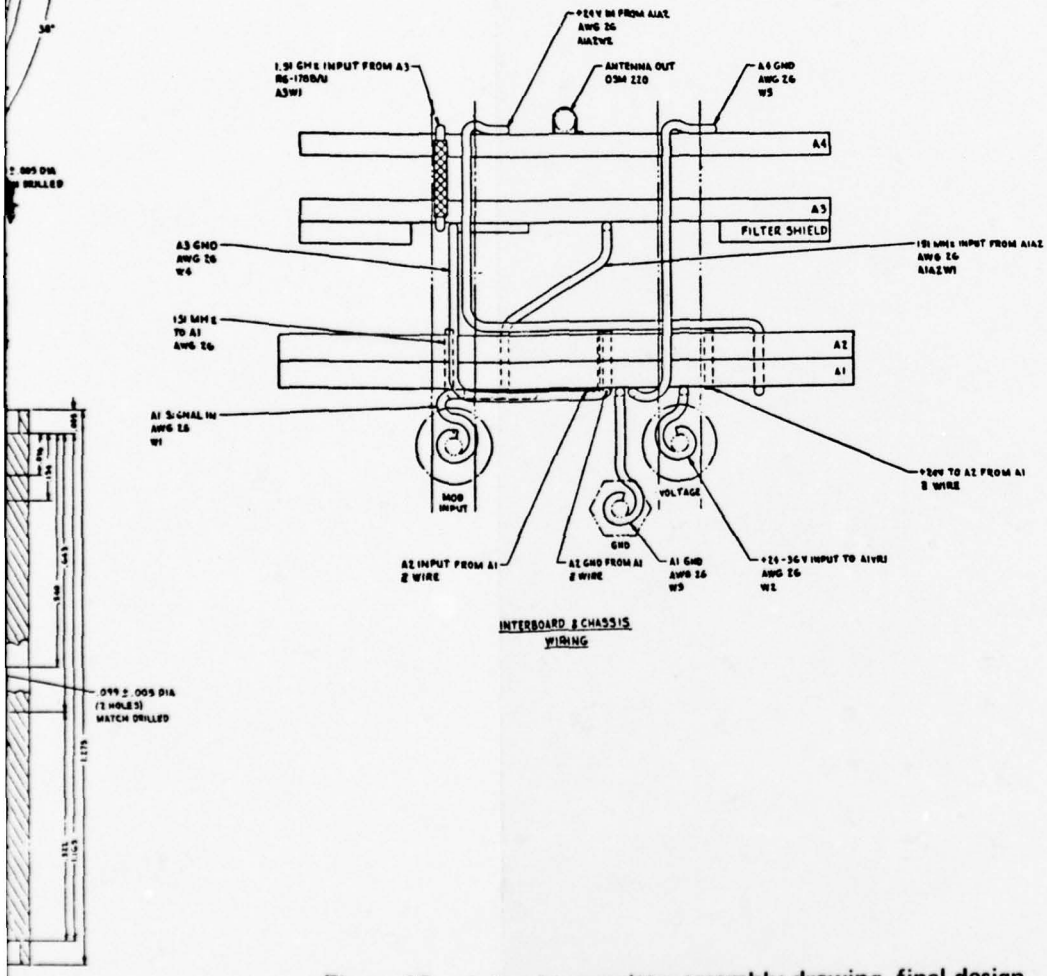
Figure 14. A2 and A3 boards after first gunfire test at 42 kg.





INTERBOARD & CHASSIS WIRING

Figure 15. L-band transmitter ass



INTERBOARD & CHASSIS WIRING

Figure 15. L-band transmitter assembly drawing, final design.

2

Figure 16. Details of numerically controlled chassis of HDL L-band crystal-controlled oscillator.

Figure 17 shows the A1 board, which is made of Pyralin. The board is populated with the components of the oscillator circuit, the buffer amplifier, and the voltage regulator. Figure 18 shows the A2 board, also made of Pyralin. This board is populated with the components of the times-2 frequency multiplier. Figure 19 shows the ceramic A4 board populated with the components of the 1.51 GHz output power amplifier. The A3 board is shown in a later section of this report (Figure 27).

6. ACCOMPLISHMENTS

6.1 Mechanical Design

The mechanical design of the L-band transmitter provided two significant contributions to performance and cost effectiveness. The alumina substrate assembly in the housing was tested in a gunfire environment after the mechanical redesign, and the results were satisfactory. Significant cost savings were realized by developing a computer program tape to produce the housing parts on numerically controlled machines. This same mechanical design could be applied directly for substituting Epsilam-10 material for the alumina/ceramic substrates now used in the design for boards A3 and A4, including the filter-cover balanced stripline. Additional cost savings would be realized, particularly for labor.

6.2 Electrical Design

Reference to Section 2.2, Specifications, will be useful for the following discussion of the oscillator, modulator, and power output amplifier. The performance of the oscillator meets all program objectives. Its frequency stability is within ±0.0013 percent over the temperature range of -40 to +60°C, as illustrated in Figure 20. This is well within the specifications of ±0.01 percent. After turn-on, the oscillator frequency is stabilized in less than 0.1 s.

The modulation frequency range has been extended at the high end from 300 to 750 kHz. The modulation index is now constant over the input frequency of 3 to 750 kHz, as shown in Figure 21. The variation of the modulation index with temperature is shown in Figure 22. The modulation distortion is 1.0 percent or less for the frequency range given above, which is much less than the 5 percent allowed by the specifications.

The power amplifier provides a nominal 100 mW output at 1.51 GHz. Variations of this output level with temperature are shown in Figure 23. The drop in output power is only 0.7 dB at -20°C and 1.4 dB at -40°C. The amplifier was tested into a 5:1 mismatch at all phase angles; it maintained a minimum rf output of 32 mW. It remained stable for all mismatched loads used during the test.

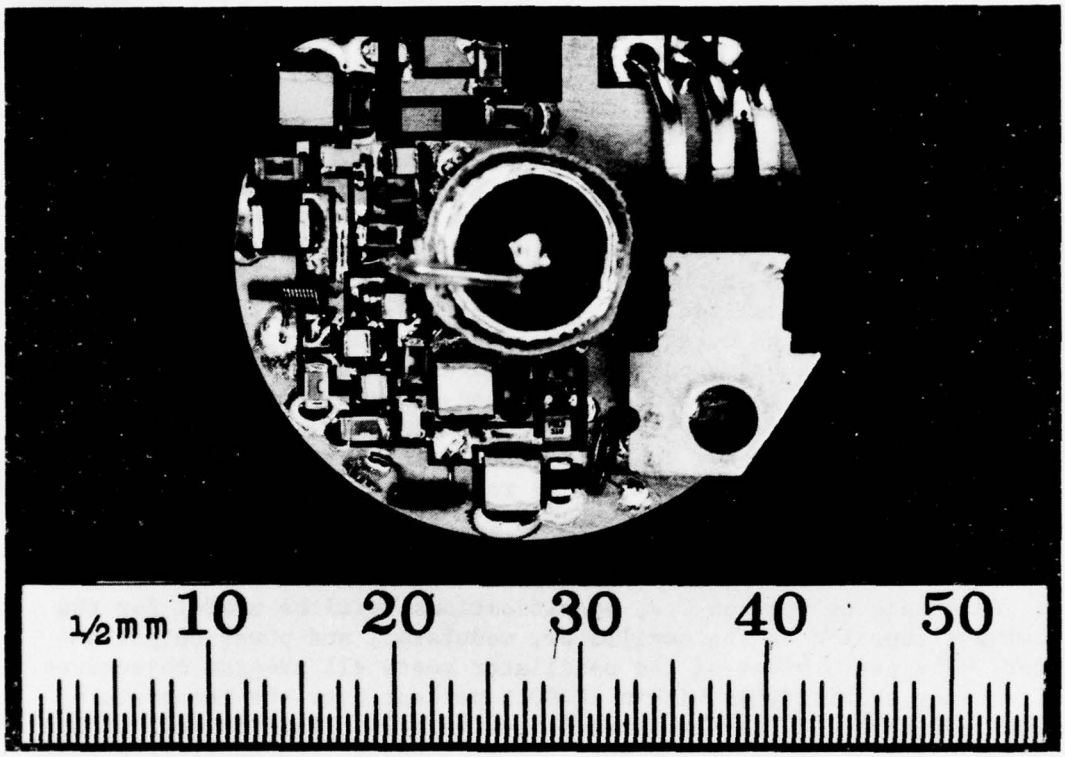


Figure 17. Assembled A1 board.

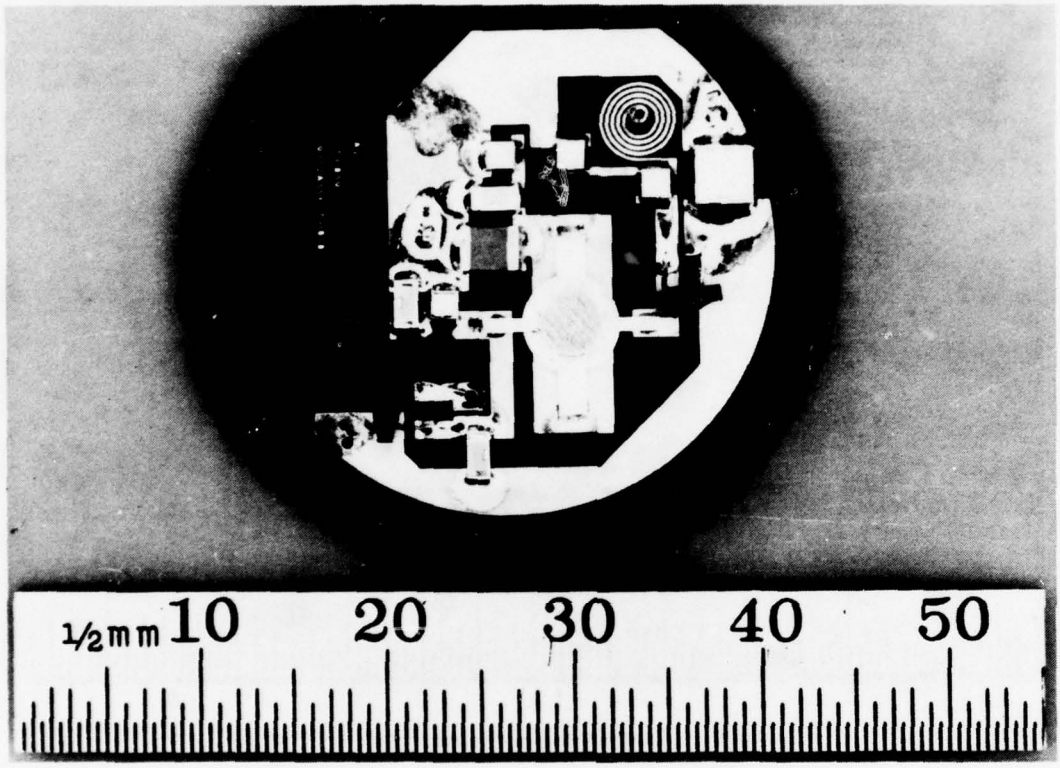


Figure 18. Assembled A2 board.

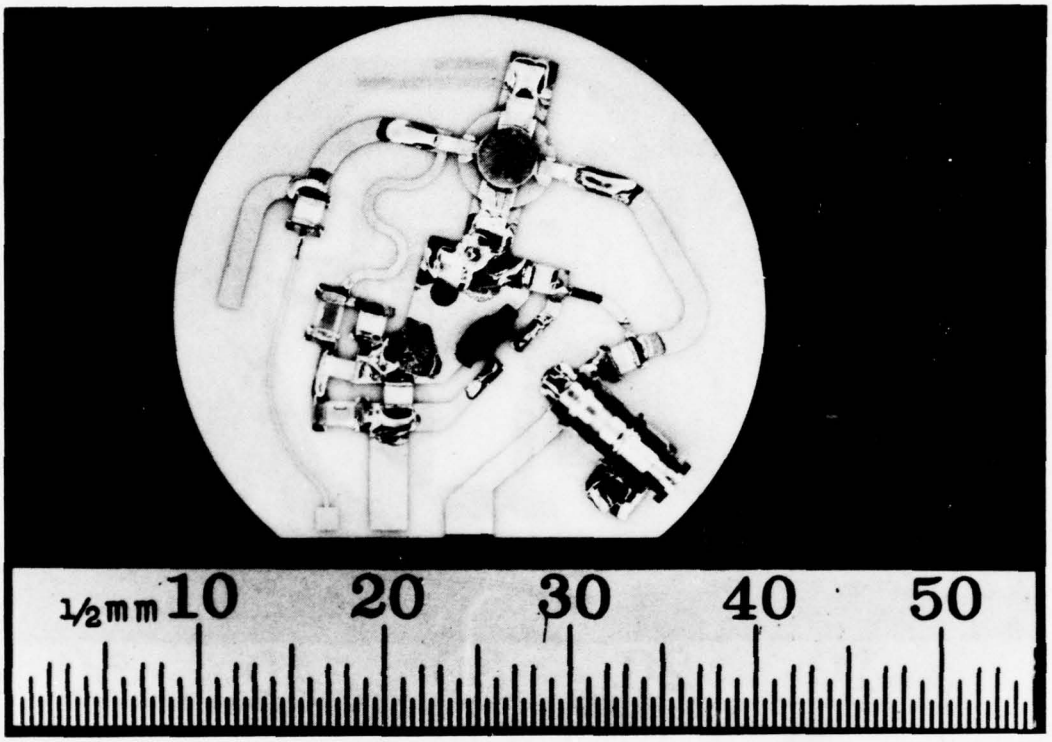


Figure 19. Assembled A4 board, ceramic substrate.

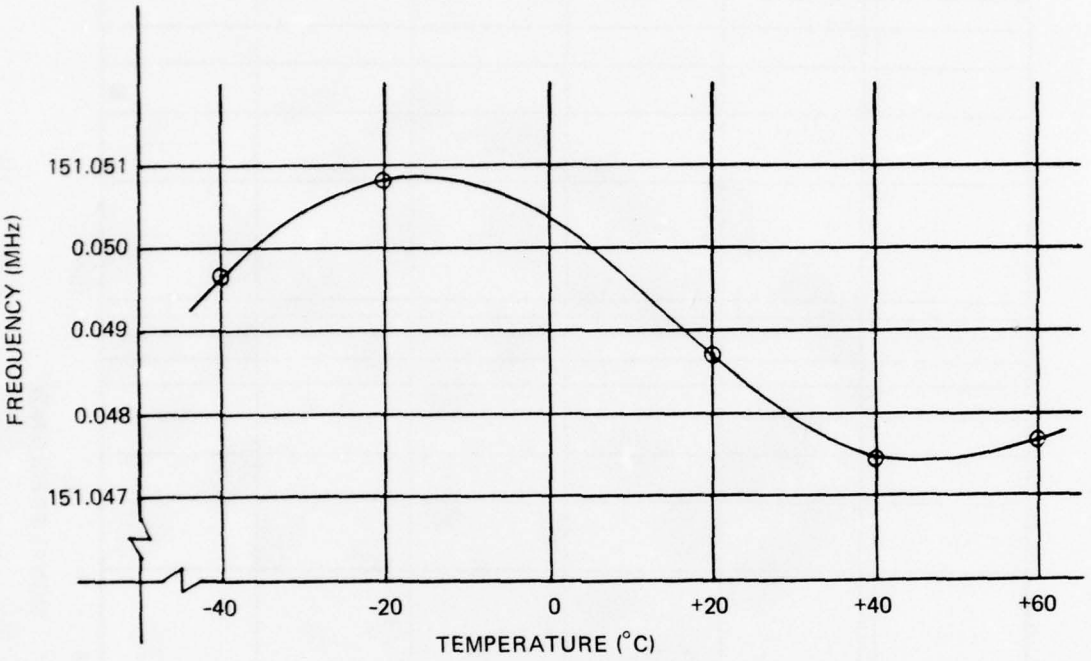


Figure 20. Oscillator frequency stability with temperature.

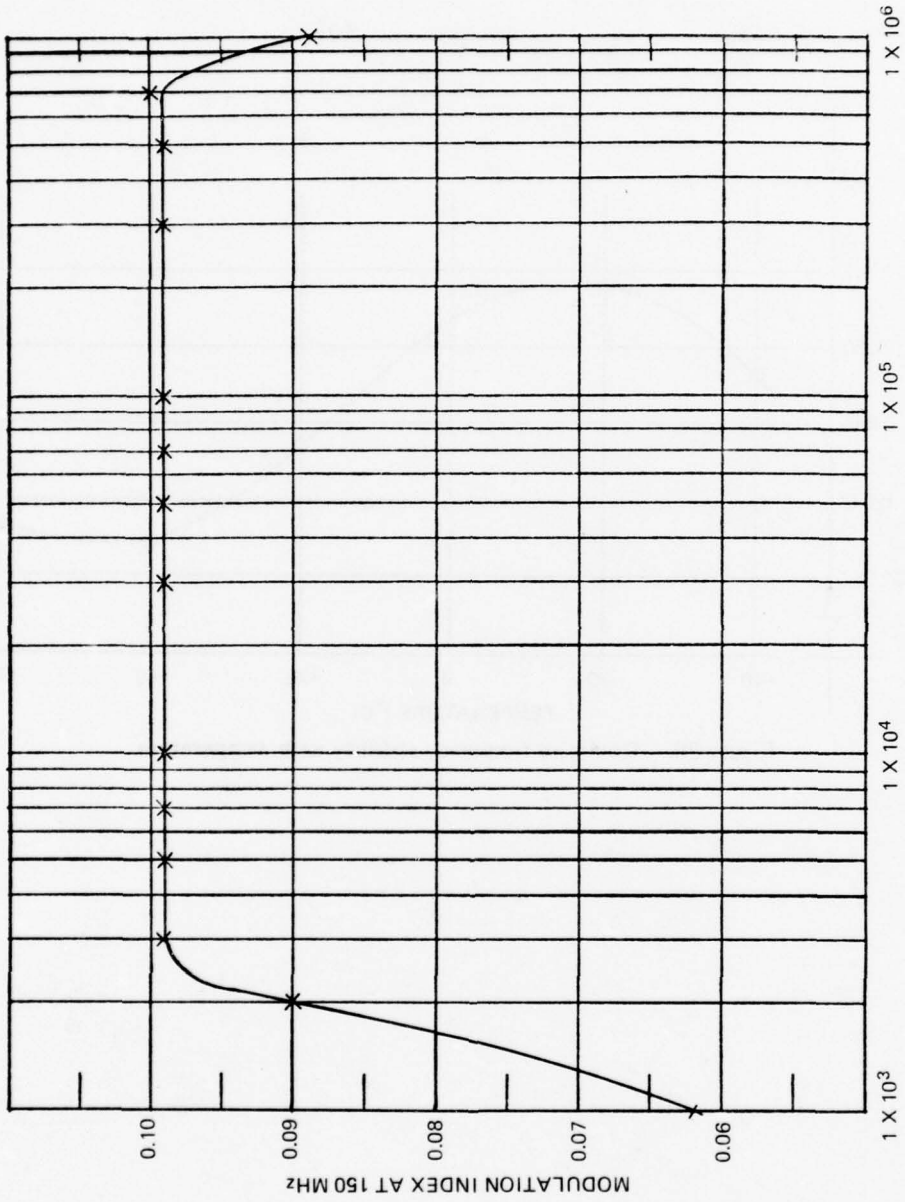


Figure 21. Modulation index as function of signal frequency.

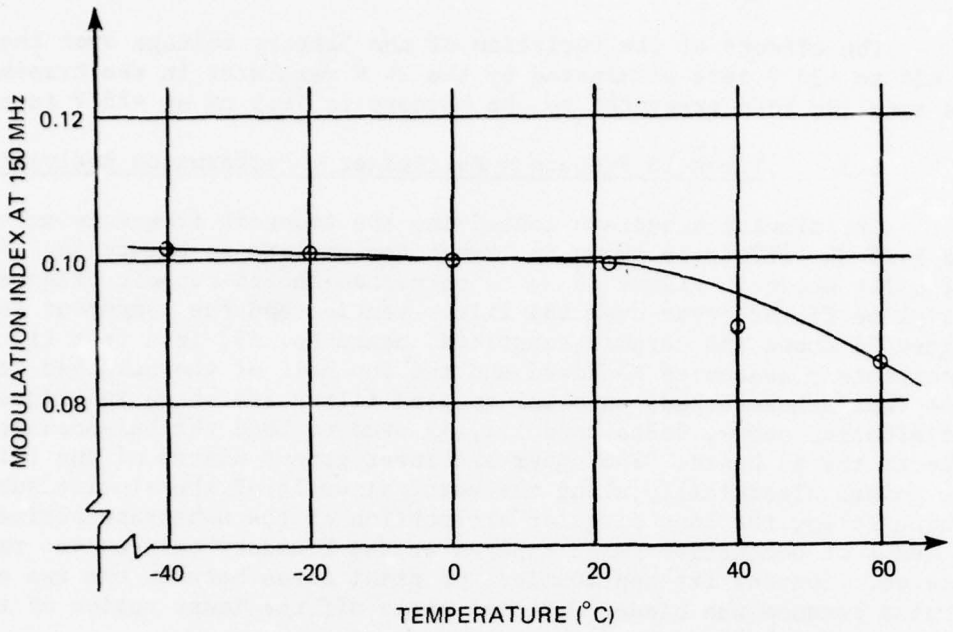


Figure 22. Modulation index variation with temperature.

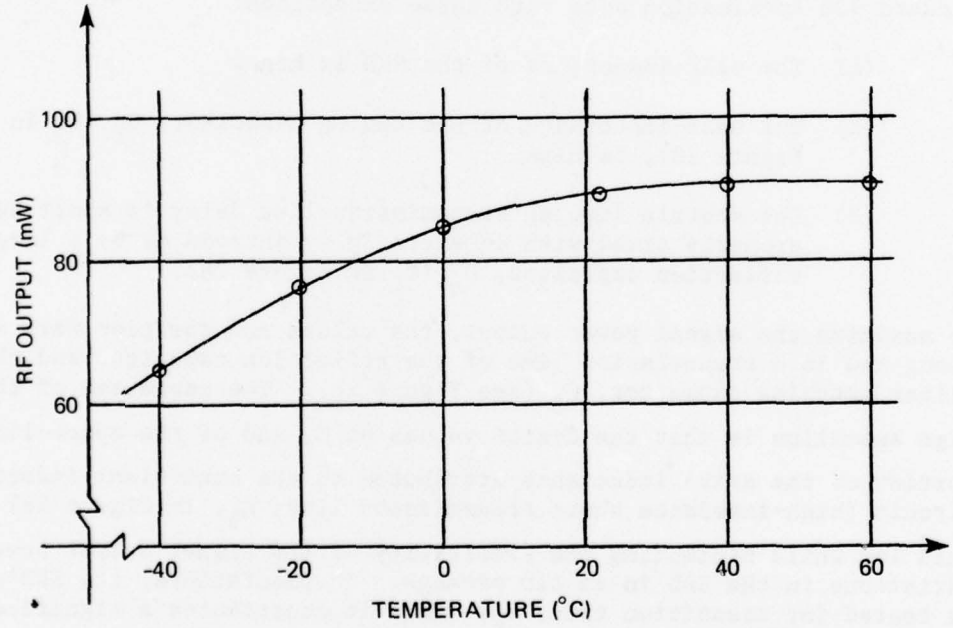


Figure 23. RF output power variation with temperature.

The effects of the variation of the battery voltage over the range of +24 to +36 V were eliminated by the 24 V regulator in the transmitter. The total dc load presented to the battery is 78.5 mA at +28 V input.

6.3 Times-10 Frequency Multiplier — Performance Analysis

The alumina substrate containing the times-10 frequency multiplier and 1.51 GHz filter is shown in layout design form in Figure 24. Schematically shown in Figure 25 is a horseshoe-shaped ceramic balanced stripline filter cover over the filter section and the component assembly. Figure 26 shows the ceramic substrate, board No. A3, in a test fixture. A completely assembled A3 board and the top half of the balanced stripline (horseshoe-shaped) parallel-coupled filter are shown in Figure 27. A dielectric epoxy, Delta Bond 152, is used to bond the balanced stripline to the A3 board. The upper and lower ground plates of the filter are joined electrically along the vertical walls of the alumina substrates (which follow the long circular arc portion of the substrate perimeter) by means of conductive paint applied at the boundary between the two substrates. (During its application, no paint oozes between the two substrates because the binder material seals off the inner region of the filter sandwich.)

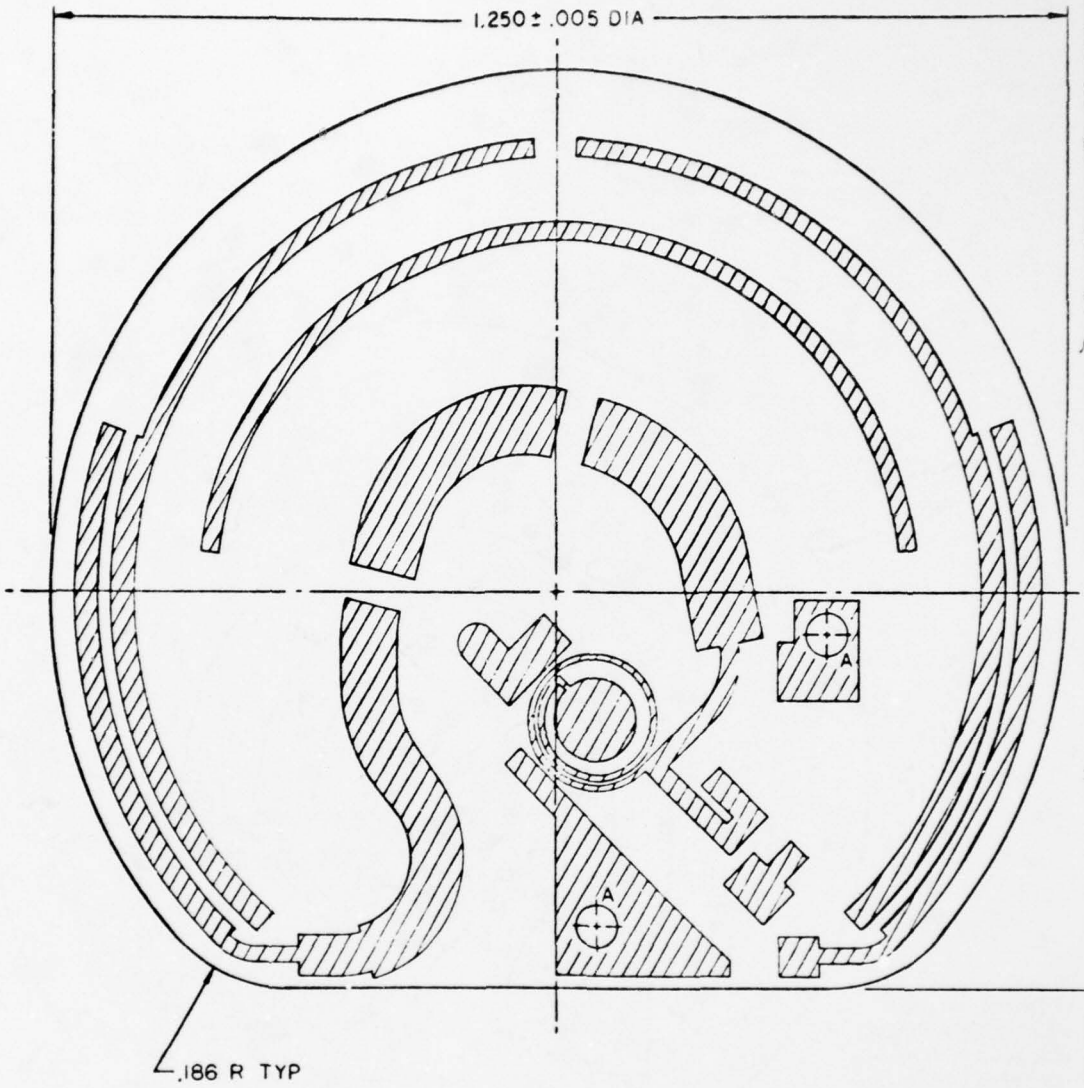
The design of the SRD resonant-line section follows the Hewlett-Packard 920 Application Note with three exceptions:

(1) The self-inductance of the SRD is high.

(2) The self-inductance of the tuning capacitor, C_T (C_3 in Figure 28), is high.

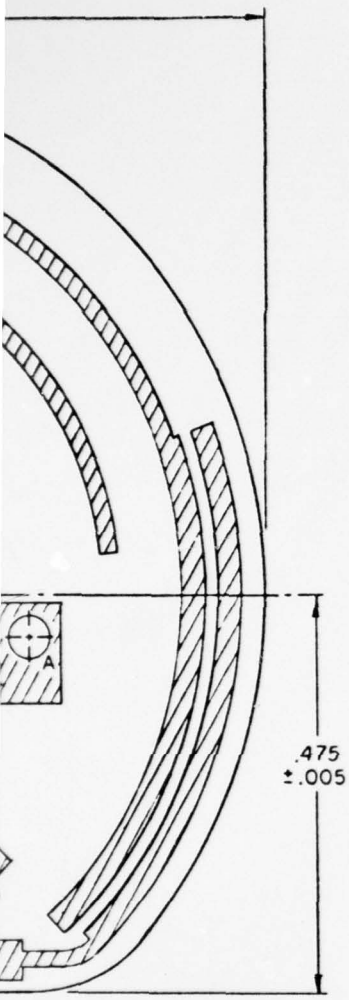
(3) The shuttle impulse transmission-line delay is short but properly timed with an extra delay introduced by a large reflection capacitor, C_c (C_4 in Figure 28).

To maximize the signal power output, the values and position were adjusted along the 38 Ω transmission line of the reflection capacitor and the post-filter matching capacitor, C_5 (see Figure 28). The advantage of the design anomalies is that the design values of C_T and of the space-limited portion of the drive inductance attributed to the equivalent inductor circuit (high-impedance short transmission line, L_3, in Figure 28) are held low while minimizing the sensitivity of the signal output power to variations in the SRD in an LID package. In manufacture, the SRD's would be tested for transition time, t_t, since it contributes a significant portion of the impulse period, t_p.



NOTES:

1- MIL-A-2550 & MIL-P-55110 APPLY.
2- MATL: .050 THK ALUMINA. 1 OZ COPPER BOTH SIDES.
3- CONDUCTOR PATTERN TO BE GOLD PLATED PER MIL-G-45204 TYPE I, CLASS 1, 50 MICRO INCHES THK.

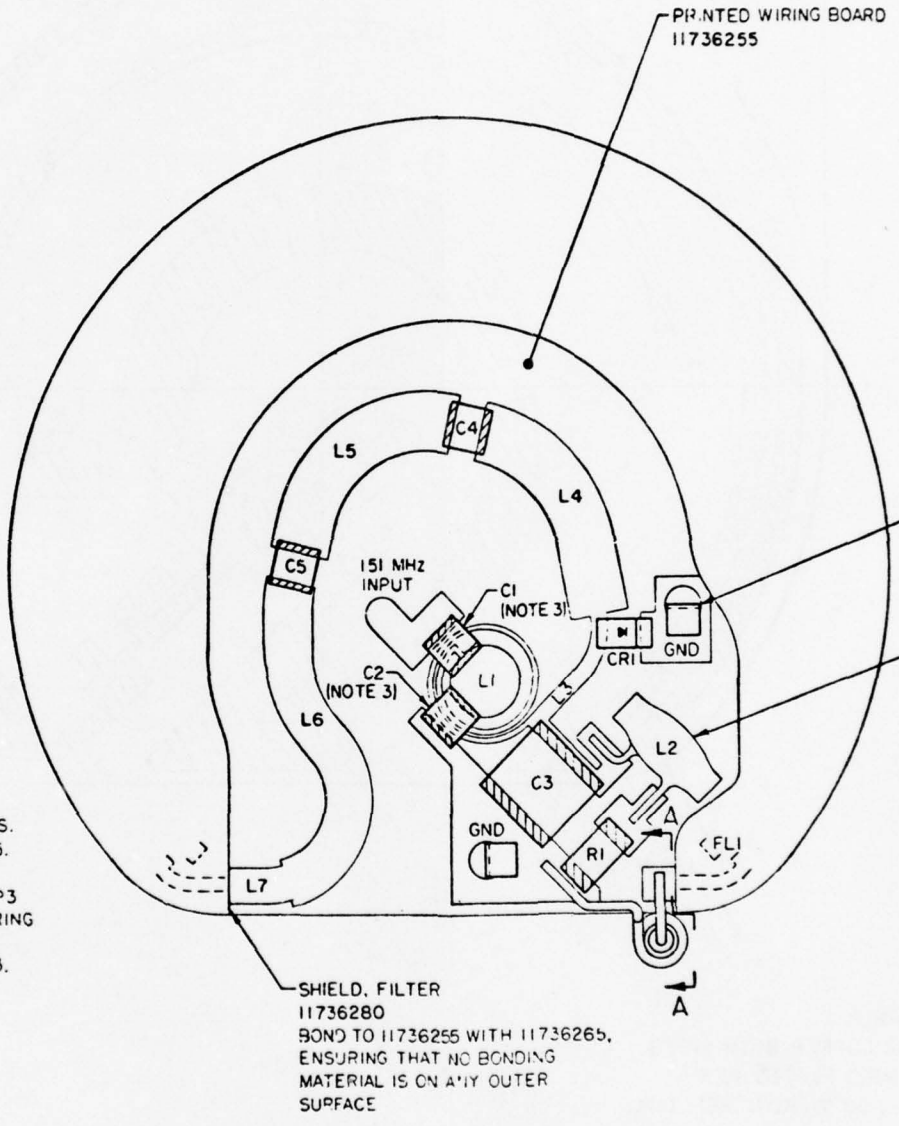


HOLE	DIAMETER	QTY
A	.052 ± .003	2

Figure 24. Basic times-10 multiplier and filter layout design.

2

REFERENCE DESIGNATION	PART NO.
C1	11736244-007
C2	11736244-013
C3	11736242-004
C4	11736244-008
C5	11736244-014
CR1	11736256
FL1	P/O BD BSC
L1	P/O BD BSC
L2	11736246-003
L3 THRU L7	P/O BD BSC
R1	11736249-002



NOTES:
1-GENERAL SPECIFICATION FOR AMMUNITION AND SPECIAL WEAPONS, MIL-A-2550, APPLIES.
2-SOLDER PER MIL-STD-454, REQUIREMENT 5.
3-C1 & C2 TO BE MOUNTED ON THEIR SIDE.
4-SOLDER ALL COMPONENTS USING SN62 WRAP3 SOLDER PER QQ-S-571. ALL OTHER SOLDERING USE SN63 WRAP4 SOLDER PER QQ-S-571.
5-FOR SCHEMATIC DIAGRAM SEE DWG 11736263.

Figure 25. Filter schematic layout de

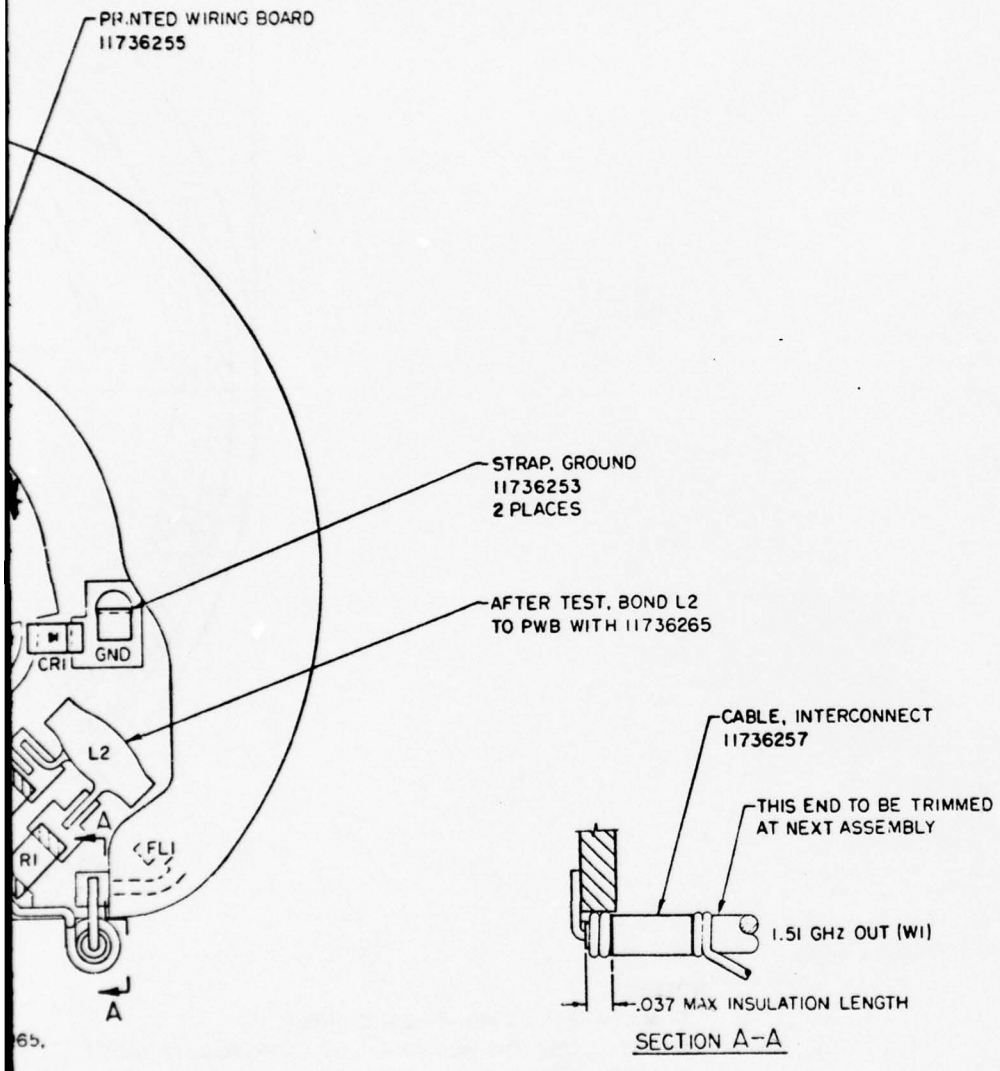


Figure 25. Filter cover and component assembly of times-10 multiplier schematic layout design.

4

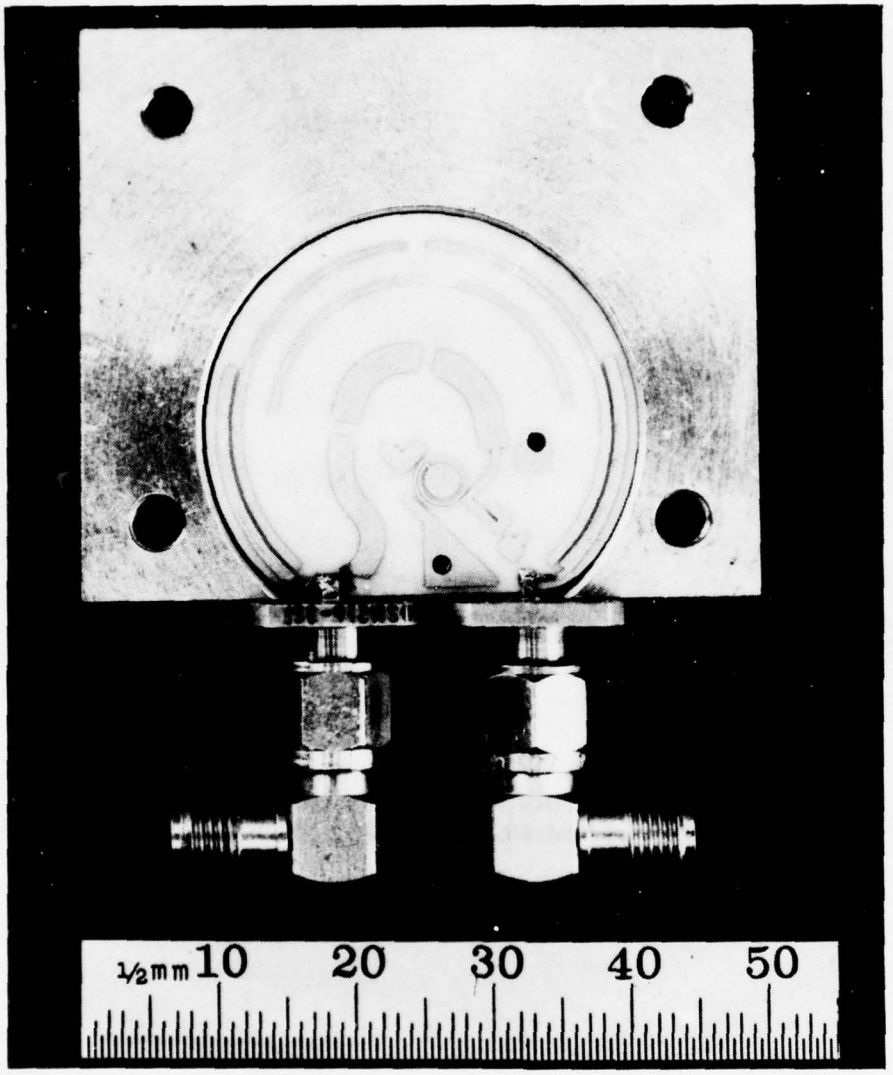


Figure 26. Ceramic substrate for L-band times-10 multiplier/filter in test fixture.

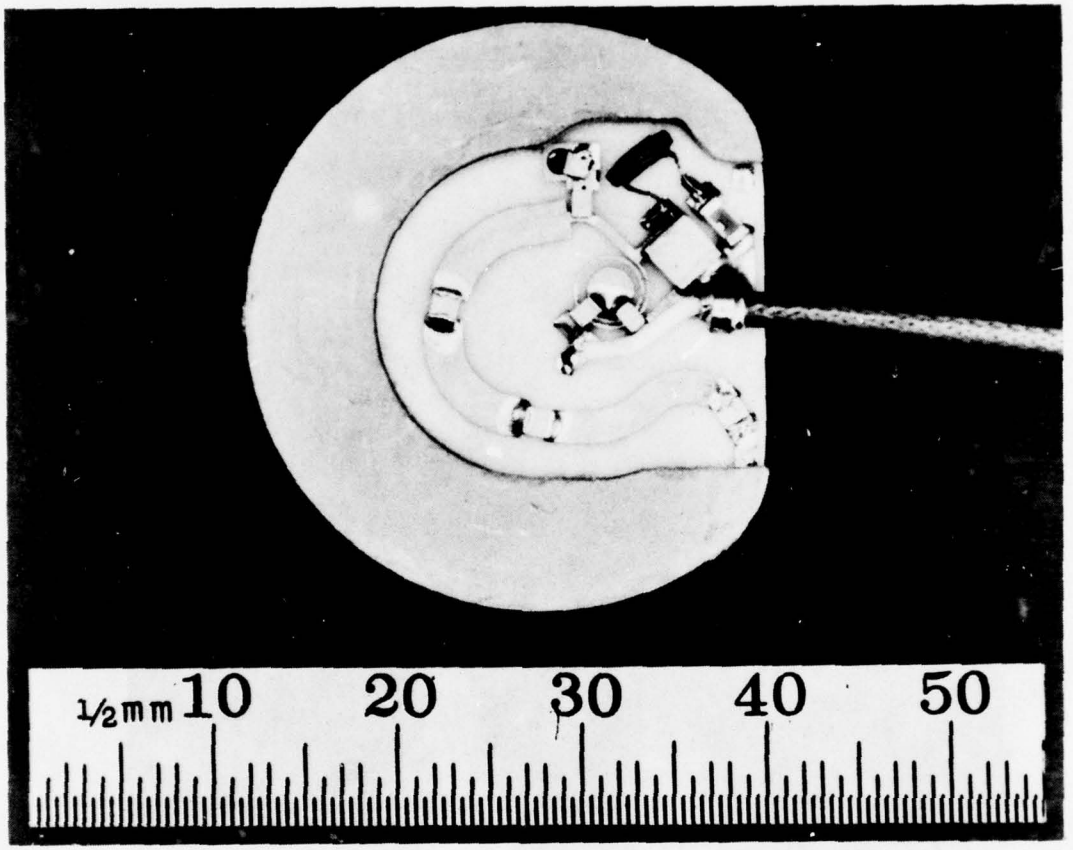


Figure 27. Assembled A3 ceramic substrate.

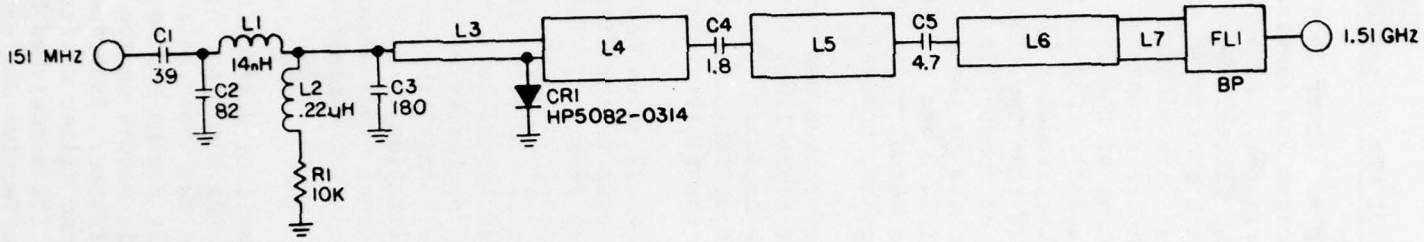


Figure 28. Schematic diagram, times-10 multiplier.

6.4 Analysis of 1.51 MHz Filter Performance

The parallel edge-coupled filter is a three-resonator Tchebysheff design that has been folded about its longest axis and bent inward to conform to a circular arc perimeter. As a result of these anomalous topological contortions of the filter, the first and last 1/2-wavelength resonator elements (F Typ) were abutted in the gap area marked 2°52' Typ in Figure 29. Therefore, they were withdrawn to open a gap to prevent bypass coupling around the middle resonator. This forced the long sections down toward the breakpoint of the flat of the D-shaped substrate (see Figure 29, locations U and T). One of the manufacturing problems is that the input/output filter launcher lines and the outer element of the coupler-line pair are less than two line widths from the electric wall that is formed by means of conductive paint. Qualitatively, this outer metallized wall is so close to the 1/4-wavelength-long couplers that an odd-mode impedance of 54 Ω can be calculated if a TEM model is assumed (see Figure 30). The actual modes of propagation are related to those found in a trough waveguide; however, they were not analyzed.

Since the filter's performance was quite different from what would be expected when a normal, straight-line, infinite-wall, balanced stripline design was realized, the empirical design approach was used. The result was that the input/output impedance was ≈26 Ω, but this value was sensitive to the position of the filter relative to the vertical walls.

The photograph in Figure 27 shows the input/output areas of the filter in some detail. The input to the filter is a transition from microstrip to balanced stripline geometry. The output suffers the discontinuities of these transitions plus another transition to coaxial geometry, in order to reach the final amplifier 187 mils away, on the other side of the floor of the upper L-band housing cylinder. Both transitions are affected by the extent of enclosure of the D-shaped substrate by the metallization along the walls forming the long circular arc portion of the perimeter. As the metallization is brought closer to the input/output launch regions, the impedance drops drastically. This effect is difficult to control and compromises the manufacturability of the 1.51 MHz filter.

The second manufacturability difficulty pertains to the effect of the binder material that secures the upper balanced stripline (horseshoe-shaped piece in Figure 31) to the lower balanced stripline section during 25 000 g shock. This assembly design approach is required for any balanced stripline filter that is placed on the same substrate with a microstrip layout of the SRD multiplier. Experimentation showed that the center frequency of the narrowband filter shifted downward from the design value because the Delta Bond 152 sandwiched between the two alumina substrates resulted in a lower effective dielectric constant than that of pure Al_2O_3.

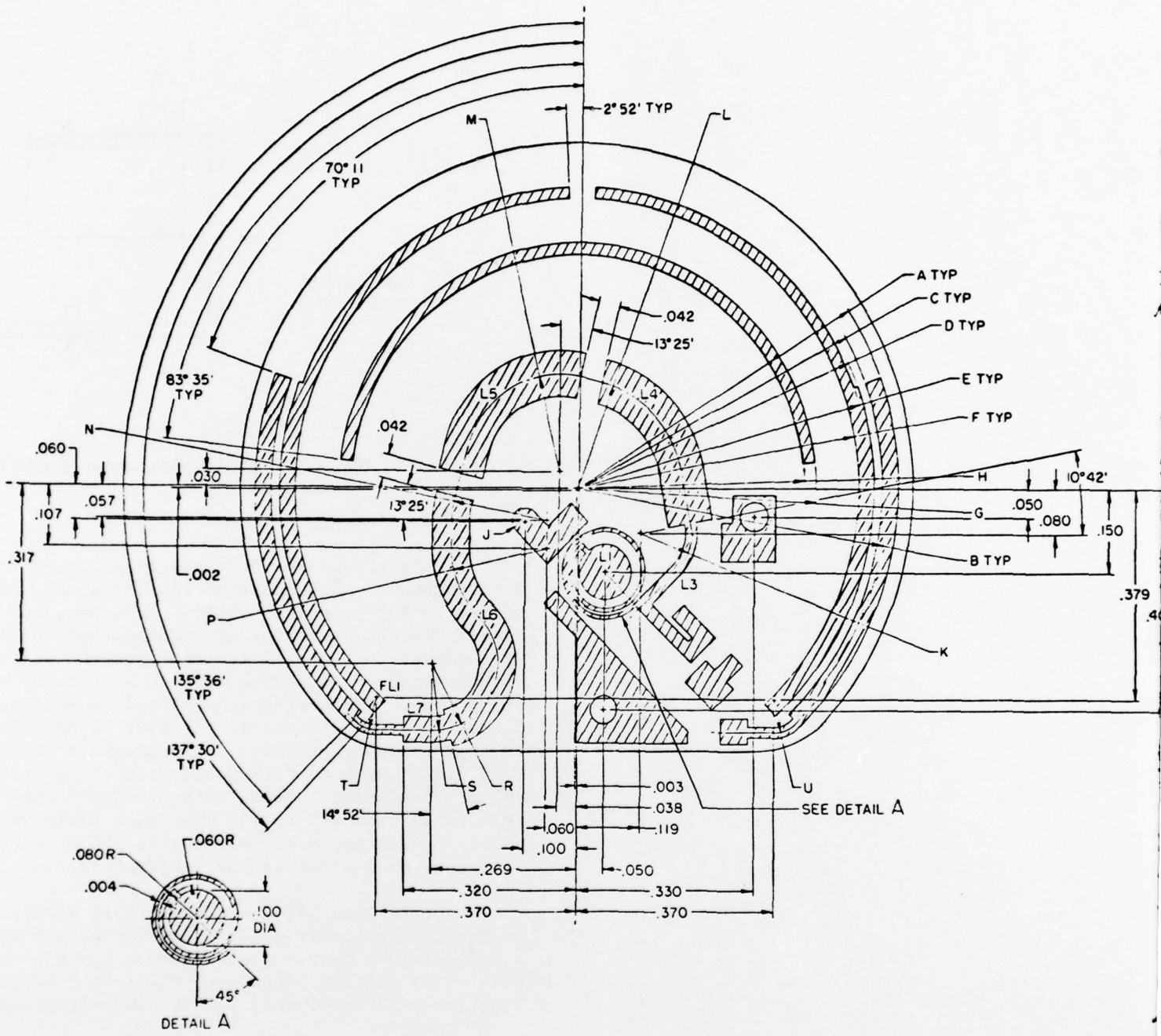
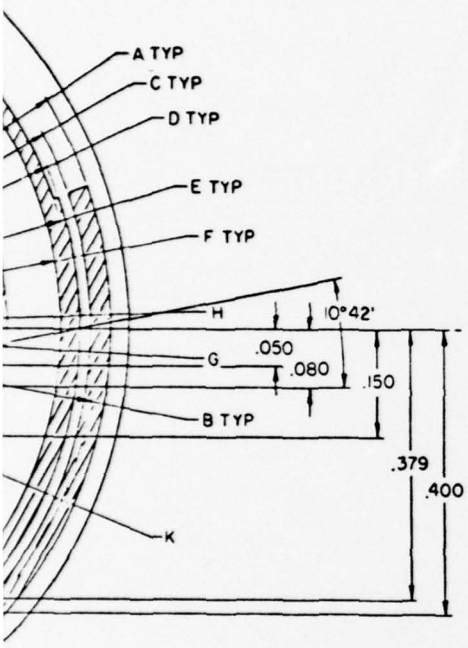


Figure 29. Di
and filter.



EE DETAIL A

SYMBOL	RADIUS	REF DES
A	.595	P/O FL1
B	.577	"
C	.566	"
D	.550	"
E	.543	"
F	.521	"
G	.443	"
H	.421	P/O FL1
J	.024	L1
K	.0936	L3
L	.200	L4
M	.175	L5
N	.175	L6
P	.175	L6
R	.120	L6
S	.120	L7
T	.059	FL1 IN
U	.059	FL1 OUT
NONE	SIZE & LOCATION OF REMAINING CNDCT PATTERN SHOWN ON SH 3	

INDUCTOR	SIZE
L1	SEE DETAIL A
L3	.0232W X .188 L
L4	.082 W X .330 L
L5	.082 W X .320 L
L6	.067 W X .480 L
L7	.048 W
FL1 IN	.018 W
FL1 OUT	.018 W

Figure 29. Dimensioned schematic layout design of times-10 multiplier and filter.

2

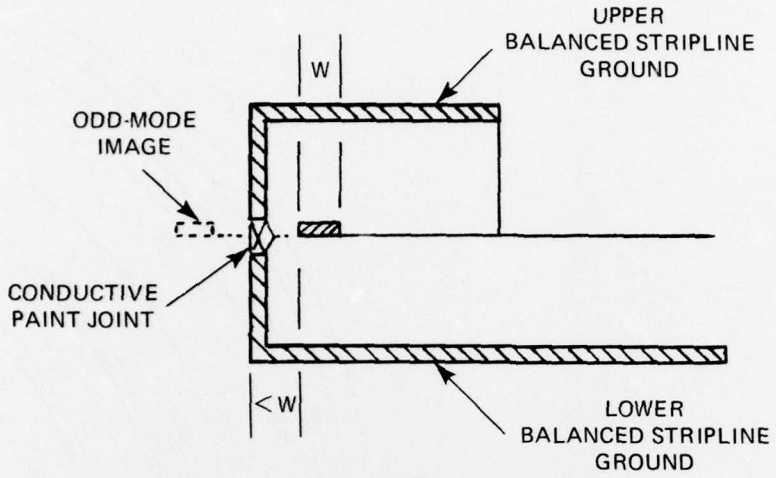


Figure 30. Odd-mode image schematic model for balanced stripline filter.

This effect was deductively analyzed to find the effective dielectric constant and Delta Bond 152 thickness, given the experimentally observed center frequency shifts. The approach used was that described by Weber[6] for the capacitor with nonhomogeneous dielectric layers. The analysis showed that the dielectric constant of Delta Bond 152 decreases from ≈6.0 at lower frequencies to ≈4.0 at L-band, assuming a binder thickness of ≈5 mils. The test specimen used to evaluate this performance had a 0.005 in. thick dielectric adhesive layer. Fabrication techniques could be used to apply pressure to reduce this dielectric thickness to about 0.001 in., which in turn would reduce the frequency shift to a tolerable value. Preliminary tests were also performed over the specified temperature range from -40 to +60°C using a filter with Delta Bond 152. The results showed that a downward shift of 10 to 20 MHz in the passband center frequency will occur as the temperature rises from -40 to +60°C.

Delta Bond 152 was a reasonable choice as a binder material because of its stable electrical properties and its bonding strength. It also has a soft-state property that allows a layer of relatively repeatable thickness to be applied. However, the effect of this bonding material in conjunction with the change in the dielectric constant of the filter substrate

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[6]Ernst Weber, Electromagnetic Theory, Dover Publications, New York, 1965. (Library of Congress Catalog No. 65-27006).

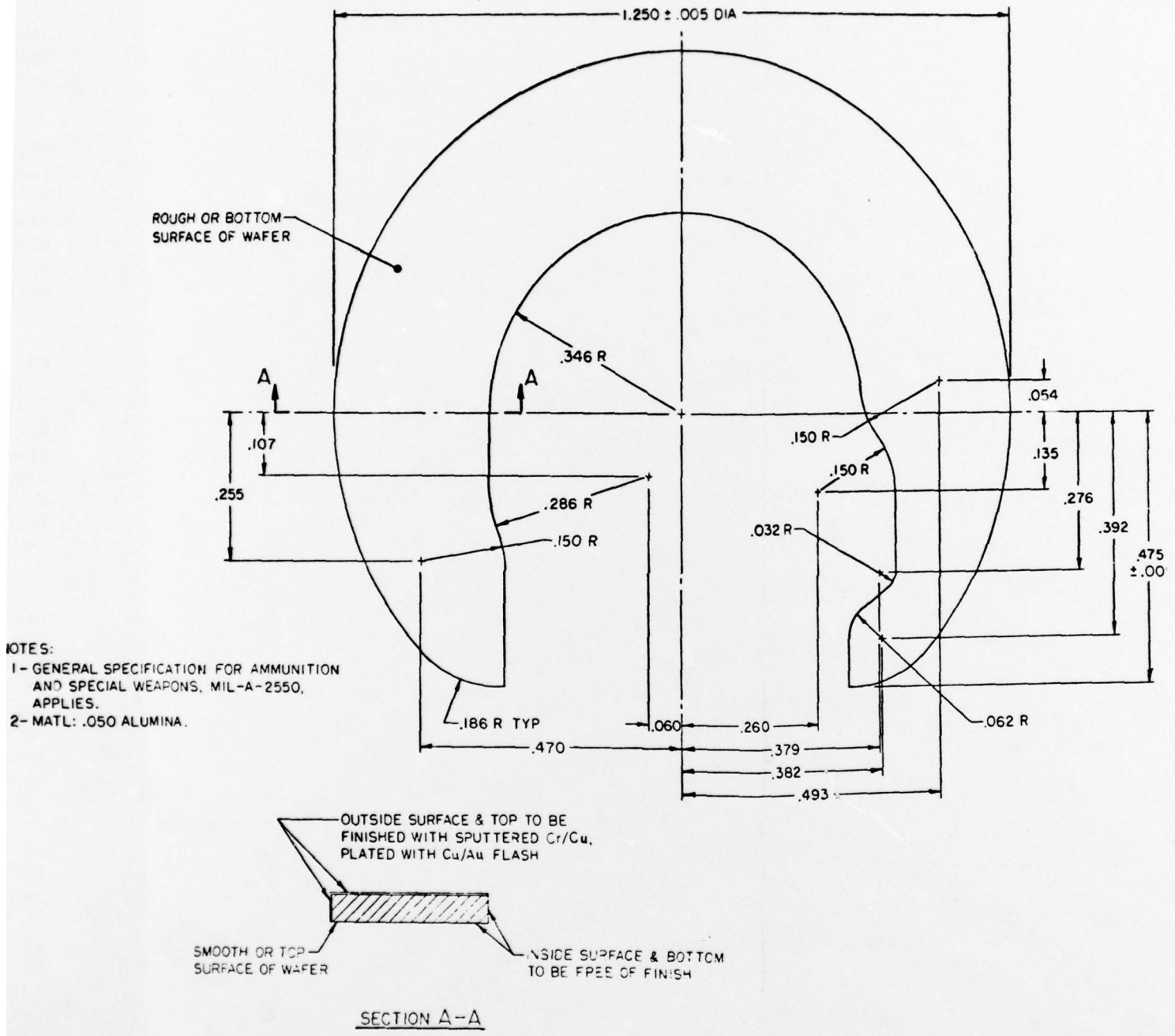

Figure 31. Upper balanced stripline filter shield.

with temperature makes it prudent to include a 4 dB filter stop-band attenuation design margin as well as some reasonable factor for the change in passband impedances of the filter as an expected thermal variance.

Finally, the only possible filter layout is along an arc concentric with the long circular arc of the substrate perimeter. This location leads to coupling to the inner region of the A3 board, which is occupied by the resonant lines of the SRD multiplier. In turn, the resonant lines are also constrained to lie on arcs concentric with the substrate perimeter. The electrical length around the edge of the circular arc portion of the D-shaped substrate perimeter is a full wavelength at 1359 MHz, which is the ninth harmonic tone of the input frequency of 151 MHz.

Tests were made separately on the output spectrum of the SRD resonant-line circuits and the stop-band attenuation of the filter, both of which were located on the same A3 board. However, when the multiplier and filter were connected, the spectrum at the output of the filter was very different from what would have been expected had the actual multiplier spectrum been passed through a truly isolated filter with the same stop-band attenuation as that measured for the on-board filter. The harmonic at 1359 MHz was 20 dB higher than expected, and the amplitude of the low-frequency feedthrough of the 151 MHz input signal (the power level of which is +20 dBm) was equal to that of the desired signal at 1510 MHz.

The resonator design of the filter needed to attenuate the adjacent harmonic tones by 38 dB in order to satisfy performance specifications. The choice of a 5 percent bandwidth-parallel-coupled filter (n = 3), with a physical layout to fit on the D-shaped substrate with a long diameter of 1.250 in., led to the wall-coupling problems and the poor "filter" isolation. These problems occurred not only because the filter produced waveguide/cavity modes of propogation but also because it diminished the area for the SRD resonant-line multiplier layout. Therefore, the lumped elements comprising the input impulse generator were located close to the filter output launching pad.

An ancillary problem that complicates the development of a manufacturable design is the low-frequency, 75 MHz oscillation, which was sensitive to loading across the 10 kΩ bias resistor and to slight changes of the input frequency. The circuit's parametric stability was not analyzed, but experimental evidence showed that it is coincidentally related to the same layout area constraint that resulted in the coupling of the input signal to the output cable leading to the final amplifier. The parametric stability problem might be solved by avoiding the proximity of the times-10 multiplier and the filter.

7. CONCLUSIONS AND RECOMMENDATIONS

7.1 Manufacturability of the A3 Board

In view of the manufacturing difficulties uncovered during testing of the A3 board and the pertinent previous analysis of the interrelated circuit design and size limitations, the APL design for the A3 "SRD, times-10 multiplier filter" board is not manufacturable. Section 7.3.1 describes a design suggestion to accommodate the fundamental required radial dimension of the cavity (but not the transmitter package's height dimension) and to desensitize the signal to the SRD multiplier/filter impedance.

7.2 Manufacturability of the A1, A2, and A4 Boards

The performance of the oscillator, modulator, times-2 frequency multiplier, and 1.51 GHz power output amplifier indicates that these portions of the L-band transmitter design are satisfactory and could be produced in quantity with a high probability of satisfying the specification requirements. The mechanical parts and the use of numerically controlled automated machining techniques should be cost effective in production. The use of Pyralin and alumina ceramic substrates should also be cost effective. However, if further development efforts should yield successful performance using Epsilam-10, RT/Duroid 6010 (a Rogers Corp. trade name for their ceramic-PTFE composite laminate), or some similar material to replace the alumina ceramic parts, a significant reduction in material and labor costs would be realized.

7.3 Redesign Considerations for the A3 Board and Its Impact on Frequency Multiplication

Difficulties experienced with the "times-10 SRD/5 percent filter" circuit indicate that a basic study to redesign this function should be given high priority. A frequency multiplication chain of times-2, times-2, times-5 is used frequently in industry as a conventional circuit element where efficiency is not critical. It was initially eliminated for this application because of the high power drain, the need for additional tuning components and trimming, and the large component sizes (which usually require more assembly housing space). However, further study of this three-stage multiplication chain may be warranted by the introduction of new materials and smaller components.

7.3.1 Possible A3 Board Redesign Approach

The basic times-2, times-10 multiplication chain was analyzed. The internal specifications of the multiplier chain were calculated, starting from the transmitter output where the specifications are fixed

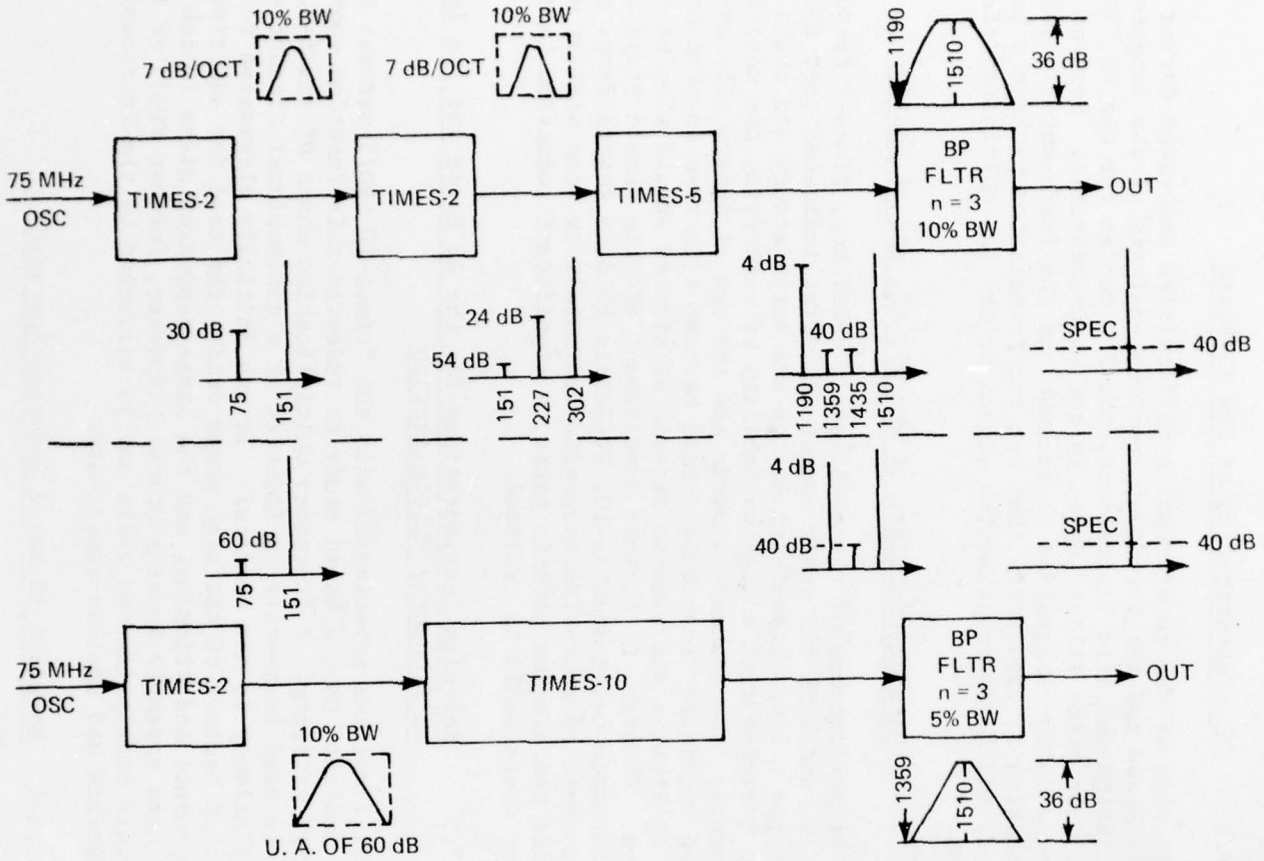

Figure 32. Comparison of multiplier chains.

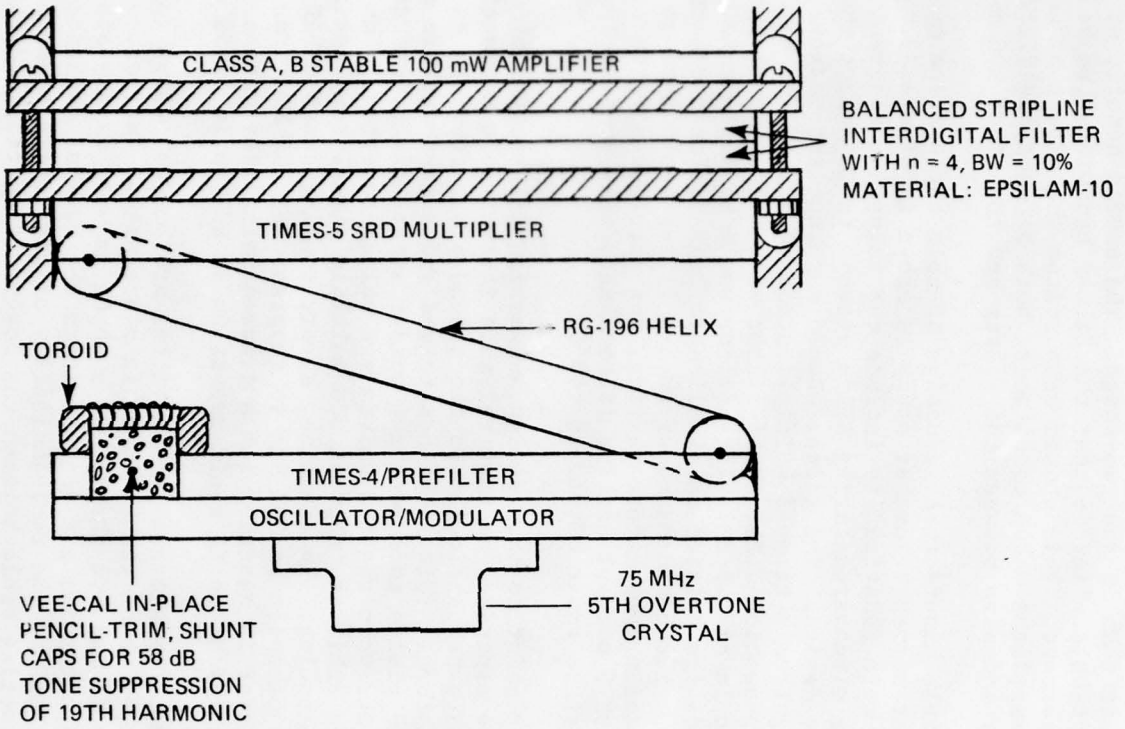

Figure 33. Alternate design for L-band transmitter.

as part of the IRIG FM telemetry link. The filtering requirements — when one compares the more gradual multiplication chain (times-2, times-2, times-5) to the chain in the present design shown in Figure 32 — are similar except that the suppression of the nineteenth tone by 40 dB at the output can be handled more gradually (30 to 40 dB per stage) in the three-stage multiplier than in the two-stage. The second benefit of choosing the times-5 SRD multiplier is that the filter bandwidth can be relaxed from 5 to 10 percent. This should help soften the effect of unpredictable intercircuit impedance-match conditions, both between the filter and the SRD multiplier and also between the filter and the final 100 mW amplifier.

A possible manufacturable design of this three-stage multiplication chain that warrants further study is shown in Figure 33. The SRD filter skirts were redefined to include the tolerance inherent in production that were discovered during APL's attempt to implement the times-10 SRD multiplier design. The filter should suppress the nearest expected tone resulting from a times-5 multiplication of 302 MHz by 44 dB. This implies a four-section Tchebysheff filter with a 10 percent bandwidth and a passband ripple of 0.1 dB. This filter would be implemented using an interdigital design printed on a malleable high-dielectric material such as Epsilam-10. The performance of such a filter would have to be determined by extensive temperature testing, but previous efforts at APL were successful with 5 percent combine filters made from Epsilam-10 and tested over a temperature range of -10 to +40°C.

The key point to this design suggestion is that the SRD multiplier and filter are separated so that reliable intercircuit connections can be made with straps perpendicular to the ground plane from the surface of one circuit to another. This is both a rugged and a reproducible approach. The Epsilam-10 yields to accept the solder/strap height internal to the stripline filter when the two halves are bolted together. The times-4 section design achieves inherent odd-multiple signal suppression by means of current balancing. In addition, a very compact tunable SRD multiplier prefilter can be built at 302 MHz to suppress the 227 MHz tone by 34 dB. Use of the filter in cascade with a times-4 multiplier with a third harmonic suppression of 24 dB would result in an S/I ratio of 58 dB.

The shunt capacitors in the filter are Vee-Cal chips (produced by Vitramon, Inc.), which can be tuned in place with a "marker." They are solid and should survive the 25 000 g shock as well as any other chip capacitor. The toroids are concentric to the Vee-Cal capacitors to save space and to improve the reproducibility of the interelement parasitics. The interconnecting cable between the lower uhf section and the upper L-band section would be formed along a helical path. The inner half of the cable's coaxial shield braid would be soldered to the thin metal plate in the spiral plane of the helix. The radial extremities of the coaxial helix fit into grooves cut in the cylindrical walls of the upper housing. This arrangement provides ground continuity from the lower section to the

upper section and also shielding of most radiation that might cross the narrow 200 mil void separating the lower uhf and the upper L-band sections. The unit requires greater height compared to the APL design because there is an extra section, 100 mils thick, that holds the stripline SRD filter. However, making the support plates thinner could be tolerated because the undue flex that cracked the alumina substrates during shock tests* would not cause the same damage with Epsilam-10, since a malleable material would not crack as easily as alumina. The conductive joint between the substrate and the ground plates and between the substrate and the chip components should be as resilient to shock as are the two lower boards in the present APL design and for which there is no support plate between the two 60 mil thick lower-section Pyralin boards.

7.3.2 Potential Advanced Technology Approaches

Recent development in voltage controlled oscillators (VCO's) have extended their frequency range upward toward 1 GHz. A 750 GHz VCO combined with a simplified times-2 multiplier stage could be considered for this application. The filtering capabilities of surface acoustic wave (SAW) devices have also been extended to frequencies in the range of 2 GHz in industry and up to 3 GHz in laboratory research. Recently, submicron photolithography and electron-beam lithography have been developed and reduced to production practice in solid-state devices for very-large-scale integrated circuits. This technology has been adopted directly to produce the fine-line features on SAW devices for higher frequencies. These developments along with some specific circuit development should provide strong potential for a new frequency-controlled transmitter design for this application.

7.4 Recommendations

Resolution of the design problems of the 1.51 GHz filter is not likely without redesign, which might evolve in three phases:

(1) A feasibility study directed toward the question of manufacturability;

(2) Evaluation of newer approaches, both for methods and materials, to accomplish frequency multiplication and filtering at these frequencies; and

(3) A production-packaging development.

*See Appendix 2 of the Motorola report.

The first phase would involve analysis and breadboarding of proof-of-principle circuits and would be closely interrelated with the other two phases. A 750 MHz VCO, SAW interdigital filter and materials such as Epsilam-10 would be evaluated to determine performance and space savings in the second phase. The final phase would study the manufacturability of the entire design for greatest yield at minimum cost.

Implementation of this redesign is recommended as an R&D effort in order to allow the necessary latitude in the evaluation of new materials, devices, and technologies that would

- Permit the crystal oscillator/modulator to be eliminated
- Give large frequency multiplication
- Reflect current capabilities in electronic design
- Not compromise performance stability.

Expertise would be required in microwave, rf, oscillator, and packaging/mechanical design for high-impact projectile environments. The minimum time scale envisioned for this effort would be 12 months.

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